

288pin ECC Unbuffered DIMM based on 4Gb E-die

78FBGA with Lead-Free & Halogen-Free
(RoHS compliant)

datasheet

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Revision History

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1.0	- First SPEC. Release	3rd Feb. 2016	-	J.Y.Lee
1.1	- Addition of 4GB line-up	28th Apr. 2016	-	J.Y.Lee
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1. DDR4 ECC Unbuffered DIMM Ordering Information

Part Number ²	Density	Organization	Component Composition ¹	Number of Rank	Height
M391A5143EB1-CPB/RC	4GB	512Mx72	512Mx8(K4A4G085WE-BC##)*9	1	31.25mm
M391A1G43EB1-CPB/RC	8GB	1Gx72	512Mx8(K4A4G085WE-BC##)*18	2	31.25mm

NOTE :

1. "##" - PB/RC

2. PB(2133Mbps 15-15-15)/RC(2400Mbps 17-17-17)

- DDR4-2400(17-17-17) is backward compatible to DDR4-2133(15-15-15)

2. Key Features

Speed	DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	Unit
	11-11-11	13-13-13	15-15-15	17-17-17	
tCK(min)	1.25	1.071	0.937	0.833	ns
CAS Latency	11	13	15	17	nCK
tRCD(min)	13.75	13.92	14.06	14.16	ns
tRP(min)	13.75	13.92	14.06	14.16	ns
tRAS(min)	35	34	33	32	ns
tRC(min)	48.75	47.92	47.06	46.16	ns

- JEDEC standard 1.2V ± 0.06V Power Supply
- V_{DDQ} = 1.2V ± 0.06V
- 800 MHz f_{CK} for 1600Mb/sec/pin, 933 MHz f_{CK} for 1866Mb/sec/pin, 1067MHz f_{CK} for 2133Mb/sec/pin, 1200MHz f_{CK} for 2400Mb/sec/pin
- 16 Banks (4 Bank Groups)
- Programmable CAS Latency: 10,11,12,13,14,15,16,17,18
- Programmable Additive Latency (Posted CAS): 0, CL - 2, or CL - 1 clock
- Programmable CAS Write Latency (CWL) = 9,11 (DDR4-1600), 10,12 (DDR4-1866), 11,14 (DDR4-2133) and 12,16 (DDR4-2400)
- Burst Length: 8, 4 with tCCD = 4 which does not allow seamless read or write [either On the fly using A12 or MRS]
- Bi-directional Differential Data Strobe
- On Die Termination using ODT pin
- Average Refresh Period 7.8us at lower then T_{CASE} 85°C, 3.9us at 85°C < T_{CASE} ≤ 95°C
- Asynchronous Reset

3. Address Configuration

Organization	Row Address	Column Address	Bank Address	Auto Precharge
512Mx8(4Gb) based Module	A0-A14	A0-A9	BA0-BA2	A10/AP

4. x72 DIMM Pin Configurations (Front side/Back side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	1.2V,NC	145	1.2V,NC	39	VSS	183	DQ25	77	VTT	221	VTT	114	VSS	258	DQ47
2	VSS	146	VREFCA	40	TDQS12_t,DQ S12_t,DM3_n, DBI3_n,NC	184	VSS	KEY				115	DQ42	259	VSS
3	DQ4	147	VSS	41	TDQS12_c,D QS12_c,NC	185	DQS3_c	78	EVENT_n	222	PARITY	116	VSS	260	DQ43
4	VSS	148	DQ5	42	VSS	186	DQS3_t	79	A0	223	VDD	117	DQ52	261	VSS
5	DQ0	149	VSS	43	DQ30	187	VSS	80	VDD	224	BA1	118	VSS	262	DQ53
6	VSS	150	DQ1	44	VSS	188	DQ31	81	BA0	225	A10/AP	119	DQ48	263	VSS
7	TDQS9_t,DQS 9_t,DM0_n,DB I0_n,NC	151	VSS	45	DQ26	189	VSS	82	RAS_n/A16	226	VDD	120	VSS	264	DQ49
8	TDQS9_c,DQ S9_c,NC	152	DQS0_c	46	VSS	190	DQ27	83	VDD	227	RFU	121	TDQS15_t,DQ S15_t,DM6_n, DBI6_n,NC	265	VSS
9	VSS	153	DQS0_t	47	CB4,NC	191	VSS	84	CS0_n	228	WE_n/A14	122	TDQS15_c,D QS15_c,NC	266	DQS6_c
10	DQ6	154	VSS	48	VSS	192	CB5,NC	85	VDD	229	VDD	123	VSS	267	DQS6_t
11	VSS	155	DQ7	49	CB0,NC	193	VSS	86	CAS_n/A15	230	NC,SAVE_n	124	DQ54	268	VSS
12	DQ2	156	VSS	50	VSS	194	CB1,NC	87	ODT0	231	VDD	125	VSS	269	DQ55
13	VSS	157	DQ3	51	TDQS17_t,DQ S17_t,DM8_n, DBI8_n,NC	195	VSS	88	VDD	232	A13	126	DQ50	270	VSS
14	DQ12	158	VSS	52	TDQS17_c,D QS17_c,NC	196	DQS8_c	89	CS1_n	233	VDD	127	VSS	271	DQ51
15	VSS	159	DQ13	53	VSS	197	DQS8_t	90	VDD	234	NC,A17	128	DQ60	272	VSS
16	DQ8	160	VSS	54	CB6,NC	198	VSS	91	ODT1	235	NC,C2	129	VSS	273	DQ61
17	VSS	161	DQ9	55	VSS	199	CB7,NC	92	VDD	236	VDD	130	DQ56	274	VSS
18	TDQS10_t,DQ S10_t,DM1_n, DBI1_n,NC	162	VSS	56	CB2,NC	200	VSS	93	C0,CS2_n,NC	237	NC,CS3_n,C1	131	VSS	275	DQ57
19	TDQS10_c,DQ S10_c,NC	163	DQS1_c	57	VSS	201	CB3,NC	94	VSS	238	SA2	132	TDQS16_t,DQ S16_t,DM7_n, DBI7_n,NC	276	VSS
20	VSS	164	DQS1_t	58	RESET_n	202	VSS	95	DQ36	239	VSS	133	TDQS16_c,D QS16_c,NC	277	DQS7_c
21	DQ14	165	VSS	59	VDD	203	CKE1	96	VSS	240	DQ37	134	VSS	278	DQS7_t
22	VSS	166	DQ15	60	CKE0	204	VDD	97	DQ32	241	VSS	135	DQ62	279	VSS
23	DQ10	167	VSS	61	VDD	205	RFU	98	VSS	242	DQ33	136	VSS	280	DQ63
24	VSS	168	DQ11	62	ACT_n	206	VDD	99	TDQS13_t,DQ S13_t,DM4_n, DBI4_n,NC	243	VSS	137	DQ58	281	VSS
25	DQ20	169	VSS	63	BG0	207	BG1	100	TDQS13_c,D QS13_c,NC	244	DQS4_c	138	VSS	282	DQ59
26	VSS	170	DQ21	64	VDD	208	ALERT_n	101	VSS	245	DQS4_t	139	SA0	283	VSS
27	DQ16	171	VSS	65	A12/BC_n	209	VDD	102	DQ38	246	VSS	140	SA1	284	VDDSPD
28	VSS	172	DQ17	66	A9	210	A11	103	VSS	247	DQ39	141	SCL	285	SDA
29	TDQS11_t,DQ S11_t,DM2_n, DBI2_n,NC	173	VSS	67	VDD	211	A7	104	DQ34	248	VSS	142	VPP	286	VPP
30	TDQS11_t,DQ S11_t,NC	174	DQS2_c	68	A8	212	VDD	105	VSS	249	DQ35	143	VPP	287	VPP
31	VSS	175	DQS2_t	69	A6	213	A5	106	DQ44	250	VSS	144	RFU	288	VPP
32	DQ22	176	VSS	70	VDD	214	A4	107	VSS	251	DQ45	NOTE: 1. Light colored text indicates functions that are not applicable for UDIMM wiring. An example is the A17 for pin 234 because UDIMMs defined by this specification will never have DIMM wiring for this pin.			
33	VSS	177	DQ23	71	A3	215	VDD	108	DQ40	252	VSS				
34	DQ18	178	VSS	72	A1	216	A2	109	VSS	253	DQ41				
35	VSS	179	DQ19	73	VDD	217	VDD	110	TDQS14_t,DQ S14_t,DM5_n, DBI5_n,NC	254	VSS				
36	DQ28	180	VSS	74	CK0_t	218	CK1_t	111	TDQS14_c,D QS14_c,NC	255	DQS5_c				
37	VSS	181	DQ29	75	CK0_c	219	CK1_c	112	VSS	256	DQS5_t				
38	DQ24	182	VSS	76	VDD	220	VDD	113	DQ46	257	VSS				

5. Pin Description

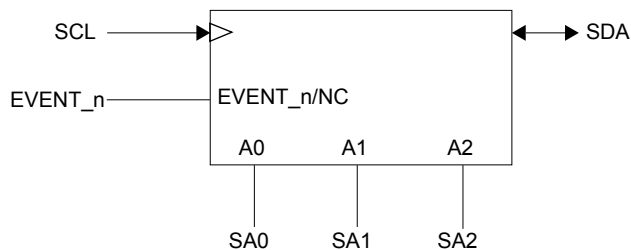
Pin Name	Description	Pin Name	Description
A0–A17 ¹	SDRAM address bus	SCL	I ² C serial bus clock for SPD-TSE
BA0, BA1	SDRAM bank select	SDA	I ² C serial bus data line for SPD-TSE
BG0, BG1	SDRAM bank group select	SA0–SA2	I ² C slave address select for SPD-TSE
RAS_n ²	SDRAM row address strobe	PARITY	SDRAM parity input
CAS_n ³	SDRAM column address strobe	VDD	SDRAM I/O and core power supply
WE_n ⁴	SDRAM write enable		
CS0_n, CS1_n	DIMM Rank Select Lines	12 V	Optional power Supply on socket but not used on UDIMM
CKE0, CKE1	SDRAM clock enable lines	VREFCA	
ODT0, ODT1	SDRAM on-die termination control lines	VSS	Power supply return (ground)
ACT_n	SDRAM activate	VDDSPD	Serial SPD-TSE positive power supply
DQ0–DQ63	DIMM memory data bus	ALERT_n	SDRAM ALERT_n
CB0–CB7	DIMM ECC check bits	VPP	SDRAM Supply
TDQS0_t–TDQS8_t TDQS0_c–TDQS8_c	Dummy loads for mixed populations of x4 based and x8 based RDIMMs. Not used on UDIMMs.		
DQS0_t–DQS8_t	SDRAM data strobes (positive line of differential pair)		
DQS0_c–DQS8_c	SDRAM data strobes (negative line of differential pair)	RESET_n	Set DRAMs to a Known State
DM0_n–DM8_n, DBI0_n–DBI8_n	SDRAM data masks/data bus inversion (x8-based x72 DIMMs)	EVENT_n	SPD signals a thermal event has occurred
CK0_t, CK1_t	SDRAM clocks (positive line of differential pair)	VTT	SDRAM I/O termination supply
CK0_c, CK1_c	SDRAM clocks (negative line of differential pair)	RFU	Reserved for future use

NOTE :

1. Address A17 is not valid for x8 and x16 based SDRAMs. For UDIMMs this connection pin is NC.
2. RAS_n is a multiplexed function with A16.
3. CAS_n is a multiplexed function with A15.
4. WE_n is a multiplexed function with A14.

6. SPD and Thermal Sensor for ECC UDIMMs

On DIMM thermal sensor will provide DRAM temperature readout through a integrated thermal sensor.



Serial PD with Thermal sensor

NOTE : 1. Rawcard D(1Rx8 ECC) and G(2Rx8 ECC) support a thermal sensor.

[Table 1] Temperature Sensor Characteristics

Grade	Range	Temperature Sensor Accuracy			Units	NOTE
		Min.	Typ.	Max.		
B	75 < Ta < 95	-	+/- 0.5	+/- 1.0	°C	-
	40 < Ta < 125	-	+/- 1.0	+/- 2.0		-
	-20 < Ta < 125	-	+/- 2.0	+/- 3.0		-
Resolution		0.25			°C /LSB	-

7. Input/Output Functional Description

Symbol	Type	Function
CK0_t, CK0_c, CK1_t, CK1_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKE0, CKE1	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates internal clock signals and device input buffers and output drivers. Taking CKE LOW provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t, CK_c, ODT and CKE, are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
CS0_n, CS1_n, CS2_n, CS3_n	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code. CS2_n and CS3_n are not used on UDIMMs.
C0, C1, C2	Input	Chip ID: Chip ID is only used for 3DS for 2,4,8 high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code. Not used on UDIMMs.
ODT0, ODT1	Input	On Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n/TDQS_t, NU/TDQS_c (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x8 configurations. For x16 configuration ODT is applied to each DQ, DQSU_t, DQSU_c, DQSL_t, DQSL_c, DMU_n, and DML_n signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
ACT_n	Input	Activation Command Input: ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15 and A14.
RAS_n/A16. CAS_n/A15. WE_n/A14	Input	Command Inputs: RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, these are Addresses like A16, A15 and A14 but for non-activation command with ACT_n High, these are Command pins for Read, Write and other command defined in command truth table.
DM_n/DBI_n/ TDQS_t, (DMU_n/ DBIU_n), (DML_n/ DBIL_n)	Input/ Output	Input Data Mask and Data Bus Inversion: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DBI_n is an input/output identifying whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if DBI_n is HIGH. TDQS is only supported in x8 SDRAM configurations. TDQS is not valid for UDIMMs.
BG0 - BG1	Input	Bank Group Inputs: BG0 - BG1 define which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. x4/x8 SDRAM configurations have BG0 and BG1. x16 based SDRAMs only have BG0.
BA0 - BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A17	Input	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions. See other rows. The address inputs also provide the op-code during Mode Register Set commands. A17 is only defined for the x4 SDRAM configuration.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / BC_n	Input	Burst Chop: A12/BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
RESET_n	CMOS Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation.
DQ	Input/ Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0-DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific data sheets to determine which DQ is used.

DQS_t, DQS_c, DQSU_t, DQSU_c, DQSL_t, DQSL_c	Input/ Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQS_t, DQSL_t and DQSU_t are paired with differential signals DQS_c, DQSL_c, and DQSU_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.
TDQS_t, TDQS_c	Output	Termination Data Strobe: TDQS_t/TDQS_c are not valid for UDIMMs.
PARITY	Input	Command and Address Parity Input: DDR4 Supports Even Parity check in DRAMs with MR setting. Once it's enabled via Register in MR5, then DRAM calculates Parity with ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, BG0-BG1, BA0-BA1, A16-A0. Input parity should be maintained at the rising edge of the clock and at the same time with command & address with CS_n LOW
ALERT_n	Output	Alert: It has multi functions such as CRC error flag, Command and Address Parity error flag as Output signal. If there is error in CRC, then ALERT_n goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then ALERT_n goes LOW for relatively long period until on going DRAM internal recovery transaction is complete. During Connectivity Test mode this pin functions as an input. Using this signal or not is dependent on the system.
RFU		Reserved for Future Use. No on DIMM electrical connection is present.
NC		No Connect: No on DIMM electrical connection is present.
VDD ¹	Supply	Power Supply: 1.2 V +/- 0.06 V
VSS	Supply	Ground
VPP	Supply	DRAM Activating Power Supply: 2.5V (2.375V min, 2.75V max)
VTT ²	Supply	Power Supply for termination of Address, Command and Control, VDD/2.
12 V	Supply	12 V supply not used on UDIMMs.
VDDSPD	Supply	Power supply used to power the I2C bus on the SPD-TSE 2.5V or 3.3V.
VREFCA	Supply	Reference voltage for CA

NOTE :

1. For PC4 VDD 1.2 V. For PC4L VDD is TBD.

2. For PC4 VTT is 0.60 V. For PC4L VTT is TBD.

7.1 Address Mirroring

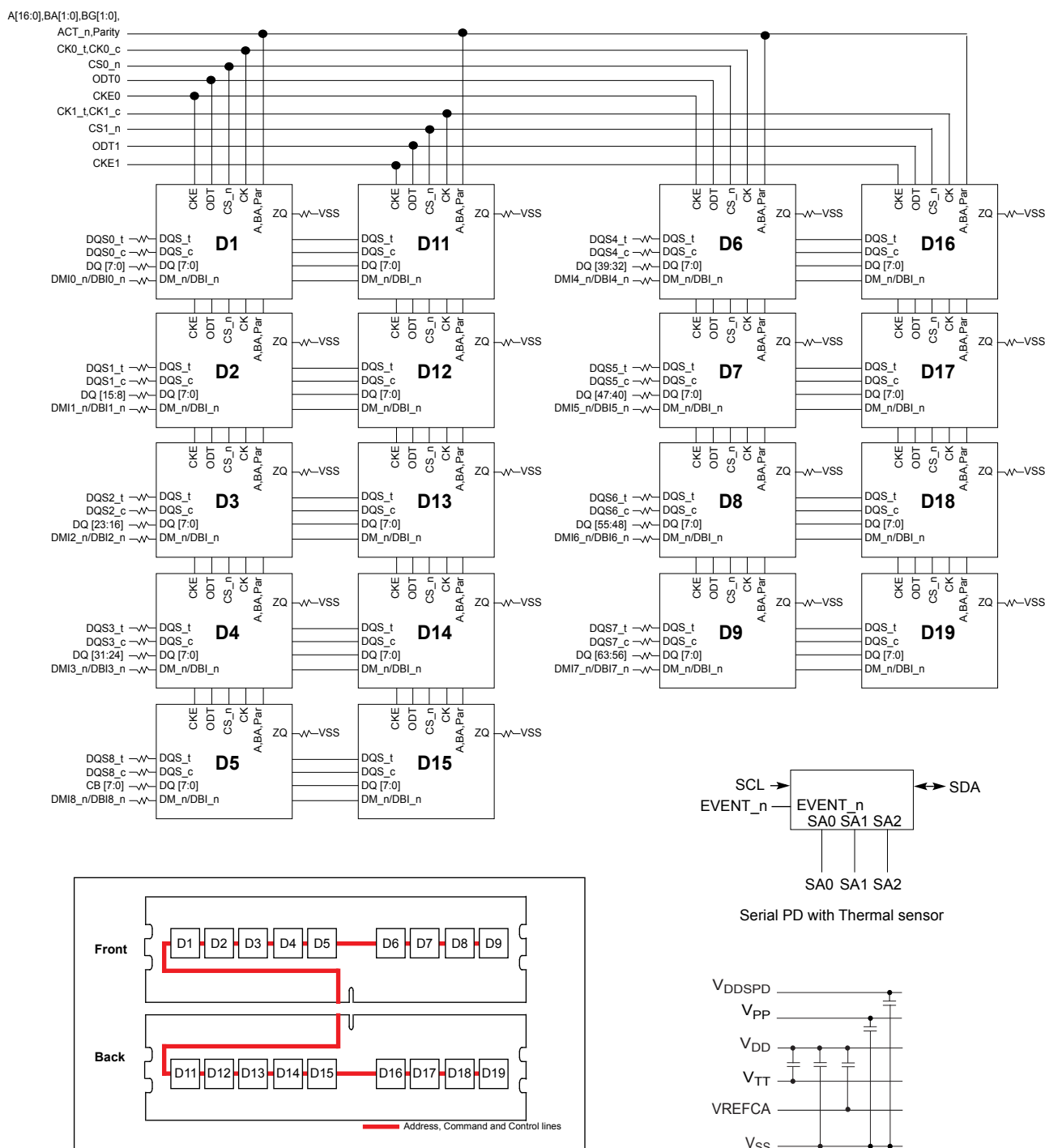
DDR4 two rank UDIMMs will use address mirroring. DRAMs for even ranks will be placed on the front side of the module. DRAMs for odd ranks will be placed on the back side of the module. Wiring of the address bus will be as defined in Table 2.

Since the cross-wired pins have no secondary functions, there is no problem in normal operation. Any data written is read the same way. There are limitations however. When writing to the internal registers with a "load mode" operation, the specific address is required. This requires the controller to know if the rank is mirrored or not. There is a bit assignment in the SPD that indicates whether the module has been designed with the mirrored feature or not. See the DDR4 SPD specification for these details. The controller must read the SPD and have the capability of de-mirroring the address when accessing the odd ranks.

[Table 2] DIMM Wiring Definition for Address Mirroring

Signal Name	DRAM Ball Label		Comment
Connector	Even Rank	Odd Rank	
A0	A0	A0	
A1	A1	A1	
A2	A2	A2	
A3	A3	A4	
A4	A4	A3	
A5	A5	A6	
A6	A6	A5	
A7	A7	A8	
A8	A8	A7	
A9	A9	A9	
A10/AP	A10/AP	A10/AP	
A11	A11	A13	
A12/BC_n	A12/BC_n	A12/BC_n	
A13	A13	A11	
A14/WE_n	A14/WE_n	A14/WE_n	
A15/CAS_n	A15/CAS_n	A15/CAS_n	
A16/RAS_n	A16/RAS_n	A16/RAS_n	
A17	A17	A17	Not valid for x8 and x16 DRAM components up to 16 Gb.
BA0	BA0	BA1	
BA1	BA1	BA0	
BG0	BG0	BG1	BG1 is not valid for x16 DRAM components. For x16 DRAM components signal BG0 will be wired to DRAM ball BG0 for both ranks.
BG1	BG1	BG0	BG1 is not valid for x16 DRAM components. For x16 DRAM components signal BG0 will be wired to DRAM ball BG0 for both ranks.

8.2 8GB, 1Gx72 ECC Module (Populated as 2 rank of x8 DDR4 SDRAMs)



NOTE :

1. Unless otherwise noted, resistor values are $15\Omega \pm 5\%$.
2. ZQ resistors are $240\Omega \pm 1\%$. For all other resistor values refer to the appropriate wiring diagram.

9. Absolute Maximum Ratings

9.1 Absolute Maximum DC Ratings

[Table 3] Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	NOTE
VDD	Voltage on VDD pin relative to Vss	-0.3 ~ 1.5	V	1,3
VDDQ	Voltage on VDDQ pin relative to Vss	-0.3 ~ 1.5	V	1,3
VPP	Voltage on VPP pin relative to Vss	-0.3 ~ 3.0	V	4
V _{IN} , V _{OUT}	Voltage on any pin except VREFCA to Vss	-0.3 ~ 1.5	V	1,3
T _{STG}	Storage Temperature	-55 to +100	°C	1,2

NOTE:

- Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
- VDD and VDDQ must be within 300 mV of each other at all times; and VREFCA must be not greater than 0.6 x VDDQ. When VDD and VDDQ are less than 500 mV; VREFCA may be equal to or less than 300 mV.
- VPP must be equal or greater than VDD/VDDQ at all times.

10. AC & DC Operating Conditions

10.1 Recommended DC Operating Conditions

[Table 4] Recommended DC Operating Conditions

Symbol	Parameter	Rating			Unit	NOTE
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.14	1.2	1.26	V	1,2,3
VDDQ	Supply Voltage for Output	1.14	1.2	1.26	V	1,2,3
VPP	Peak-to-Peak Voltage	2.375	2.5	2.75	V	3

NOTE:

- Under all conditions V_{DDQ} must be less than or equal to V_{DD}.
- V_{DDQ} tracks with V_{DD}. AC parameters are measured with V_{DD} and V_{DDQ} tied together.
- DC bandwidth is limited to 20MHz.

11. AC & DC Input Measurement Levels

11.1 AC & DC Logic Input Levels for Single-Ended Signals

[Table 5] Single-ended AC & DC Input Levels for Command and Address

Symbol	Parameter	DDR4-1600/1866/2133/2400		Unit	NOTE
		Min.	Max.		
$V_{IH,CA}(DC75)$	DC input logic high	$V_{REFCA} + 0.075$	V_{DD}	V	
$V_{IL,CA}(DC75)$	DC input logic low	V_{SS}	$V_{REFCA} - 0.075$	V	
$V_{IH,CA}(AC100)$	AC input logic high	$V_{REF} + 0.1$	Note 2	V	1
$V_{IL,CA}(AC100)$	AC input logic low	Note 2	$V_{REF} - 0.1$	V	1
$V_{REFCA}(DC)$	Reference Voltage for ADD, CMD inputs	$0.49 \cdot V_{DD}$	$0.51 \cdot V_{DD}$	V	2,3

NOTE:

1. See "Overshoot and Undershoot Specifications" on section.
2. The AC peak noise on V_{REFCA} may not allow V_{REFCA} to deviate from $V_{REFCA}(DC)$ by more than $\pm 1\% V_{DD}$ (for reference: approx. $\pm 12mV$)
3. For reference: approx. $V_{DD}/2 \pm 12mV$

11.2 AC and DC Input Measurement Levels : V_{REF} Tolerances.

The DC-tolerance limits and ac-noise limits for the reference voltages V_{REFCA} is illustrated in Figure 1. It shows a valid reference voltage $V_{REF}(t)$ as a function of time. (V_{REF} stands for V_{REFCA}).

$V_{REF}(DC)$ is the linear average of $V_{REF}(t)$ over a very long period of time (e.g. 1 sec). This average has to meet the min/max requirement in Table 5. Furthermore $V_{REF}(t)$ may temporarily deviate from $V_{REF}(DC)$ by no more than $\pm 1\% V_{DD}$.

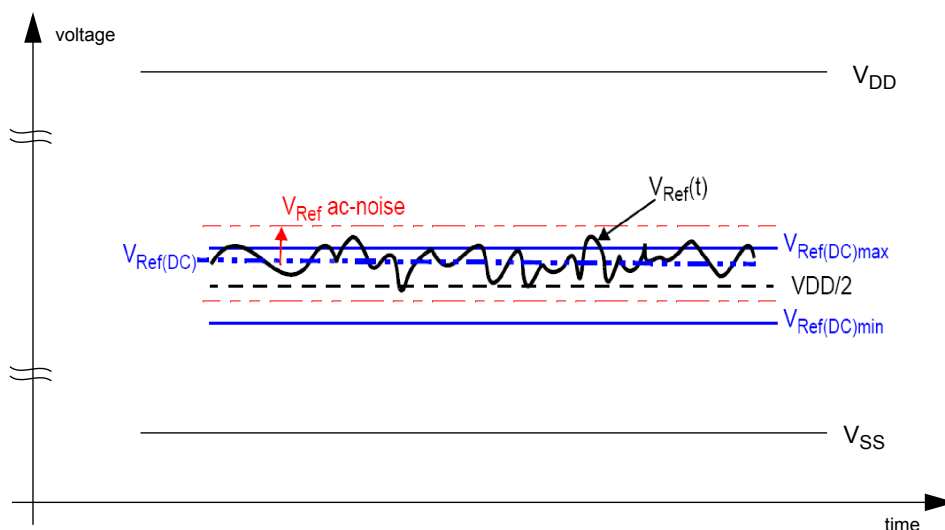


Figure 1. Illustration of $V_{REF}(DC)$ tolerance and V_{REF} AC-noise limits

The voltage levels for setup and hold time measurements $V_{IH}(AC)$, $V_{IH}(DC)$, $V_{IL}(AC)$ and $V_{IL}(DC)$ are dependent on V_{REF} .

" V_{REF} " shall be understood as $V_{REF}(DC)$, as defined in Figure 1.

This clarifies, that DC-variations of V_{REF} affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for $V_{REF}(DC)$ deviations from the optimum position within the data-eye of the input signals.

This also clarifies that the DRAM setup/hold specification and derating values need to include time and voltage associated with V_{REF} AC-noise. Timing and voltage effects due to AC-noise on V_{REF} up to the specified limit ($\pm 1\%$ of V_{DD}) are included in DRAM timings and their associated deratings.

11.3 AC and DC Logic Input Levels for Differential Signals

11.3.1 Differential Signals Definition

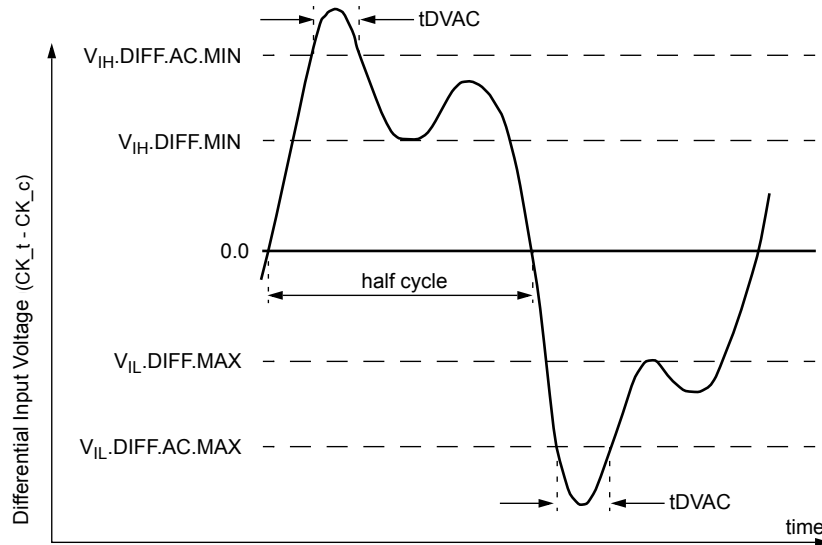


Figure 2. Definition of differential ac-swing and “time above ac-level” t_{DVAC}

NOTE:

1. Differential signal rising edge from $V_{IL,DIFF,MAX}$ to $V_{IH,DIFF,MIN}$ must be monotonic slope.
2. Differential signal falling edge from $V_{IH,DIFF,MIN}$ to $V_{IL,DIFF,MAX}$ must be monotonic slope.

11.3.2 Differential Swing Requirements for Clock ($CK_t - CK_c$)

[Table 6] Differential AC and DC Input Levels

Symbol	Parameter	DDR4 -1600/1866/2133		DDR4 -2400		unit	NOTE
		min	max	min	max		
$V_{IH,DIFF}$	differential input high	+0.150	NOTE 3	TBD	NOTE 3	V	1
$V_{IL,DIFF}$	differential input low	NOTE 3	-0.150	NOTE 3	TBD	V	1
$V_{IH,DIFF}(AC)$	differential input high ac	$2 \times (V_{IH}(AC) - V_{REF})$	NOTE 3	$2 \times (V_{IH}(AC) - V_{REF})$	NOTE 3	V	2
$V_{IL,DIFF}(AC)$	differential input low ac	NOTE 3	$2 \times (V_{IL}(AC) - V_{REF})$	NOTE 3	$2 \times (V_{IL}(AC) - V_{REF})$	V	2

NOTE:

1. Used to define a differential signal slew-rate.
2. for $CK_t - CK_c$ use $V_{IH,CA}/V_{IL,CA}(AC)$ of ADD/CMD and V_{REFCA} .
3. These values are not defined; however, the differential signals $CK_t - CK_c$, need to be within the respective limits ($V_{IH,CA}(DC)$ max, $V_{IL,CA}(DC)$ min) for single-ended signals as well as the limitations for overshoot and undershoot.

[Table 7] Allowed Time Before Ringback (t_{DVAC}) for $CK_t - CK_c$

Slew Rate [V/ns]	t_{DVAC} [ps] @ $ V_{IH/L,DIFF}(AC) = 200mV$	
	min	max
> 4.0	120	-
4.0	115	-
3.0	110	-
2.0	105	-
1.8	100	-
1.6	95	-
1.4	90	-
1.2	85	-
1.0	80	-
< 1.0	80	-

11.3.3 Single-ended Requirements for Differential Signals

Each individual component of a differential signal (CK_t, CK_c) has also to comply with certain requirements for single-ended signals.

CK_t and CK_c have to approximately reach V_{SEHmin} / V_{SELmax} (approximately equal to the ac-levels (V_{IH.CA(AC)} / V_{IL.CA(AC)}) for ADD/CMD signals) in every half-cycle.

Note that the applicable ac-levels for ADD/CMD might be different per speed-bin etc. E.g., if Different value than V_{IH.CA(AC100)}/V_{IL.CA(AC100)} is used for ADD/CMD signals, then these ac-levels apply also for the single-ended signals CK_t and CK_c

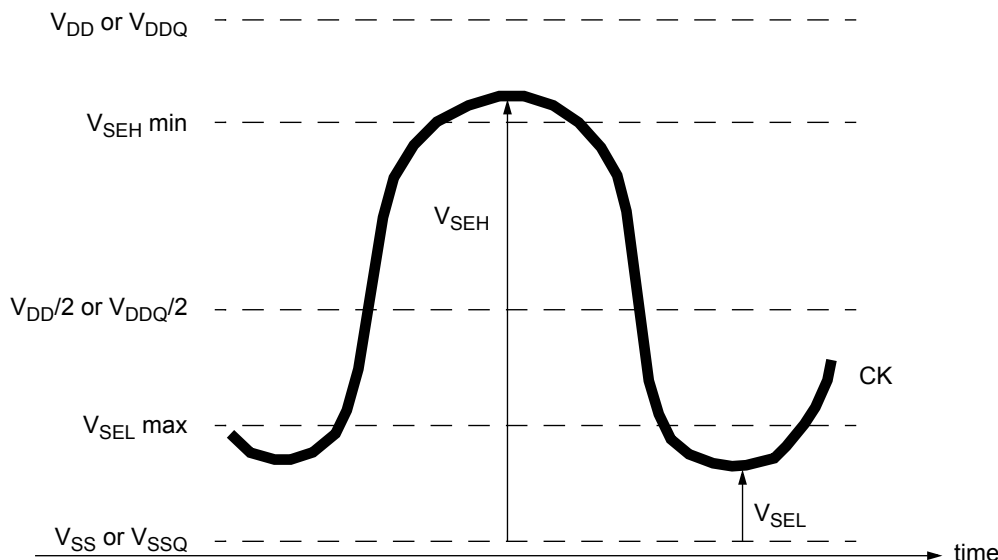


Figure 3. Single-ended requirement for differential signals.

Note that, while ADD/CMD signal requirements are with respect to V_{refCA}, the single-ended components of differential signals have a requirement with respect to V_{DD} / 2; this is nominally the same. The transition of single-ended signals through the ac-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach V_{SELmax}, V_{SEHmin} has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

[Table 8] Single-ended Levels for CK_t, CK_c

Symbol	Parameter	DDR4-1600/1866/2133		DDR4-2400		Unit	NOTE
		Min	Max	Min	Max		
V _{SEH}	Single-ended high-level for CK _t , CK _c	(V _{DD} /2)+0.100	NOTE3	TBD	NOTE3	V	1, 2
V _{SEL}	Single-ended low-level for CK _t , CK _c	NOTE3	(V _{DD} /2)-0.100	NOTE3	TBD	V	1, 2

NOTE:

1. For CK_t - CK_c use V_{IH.CA}/V_{IL.CA(AC)} of ADD/CMD;
2. V_{IH(AC)}/V_{IL(AC)} for ADD/CMD is based on V_{REFCA};
3. These values are not defined, however the single-ended signals CK_t - CK_c need to be within the respective limits (V_{IH.CA(DC)} max, V_{IL.CA(DC)}min) for single-ended signals as well as the limitations for overshoot and undershoot.

11.4 Slew Rate Definitions

11.4.1 Slew Rate Definitions for Differential Input Signals (CK)

[Table 9] Differential Input Slew Rate Definition

Description			Defined by
	from	to	
Differential input slew rate for rising edge(CK_t - CK_c)	$V_{ILdiffmax}$	$V_{IHdiffmin}$	$[V_{IHdiffmin} - V_{ILdiffmax}] / \Delta TR_{diff}$
Differential input slew rate for falling edge(CK_t - CK_c)	$V_{IHdiffmin}$	$V_{ILdiffmax}$	$[V_{IHdiffmin} - V_{ILdiffmax}] / \Delta TF_{diff}$
NOTE: The differential signal (i.e.,CK_t - CK_c) must be linear between these thresholds.			

NOTE: The differential signal (i.e., CK_t - CK_c) must be linear between these thresholds.

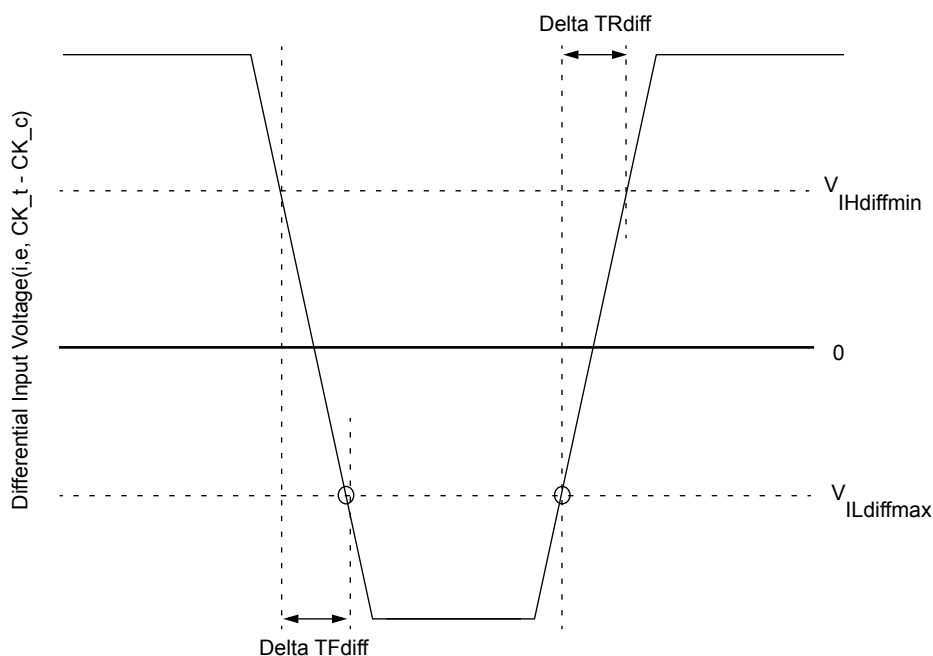


Figure 4. Differential Input Slew Rate Definition for CK_t, CK_c

11.5 Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock, each cross point voltage of differential input signals (CK_t, CK_c) must meet the requirements in Table. The differential input cross point voltage VIX is measured from the actual cross point of true and complement signals to the midlevel between of VDD and VSS.

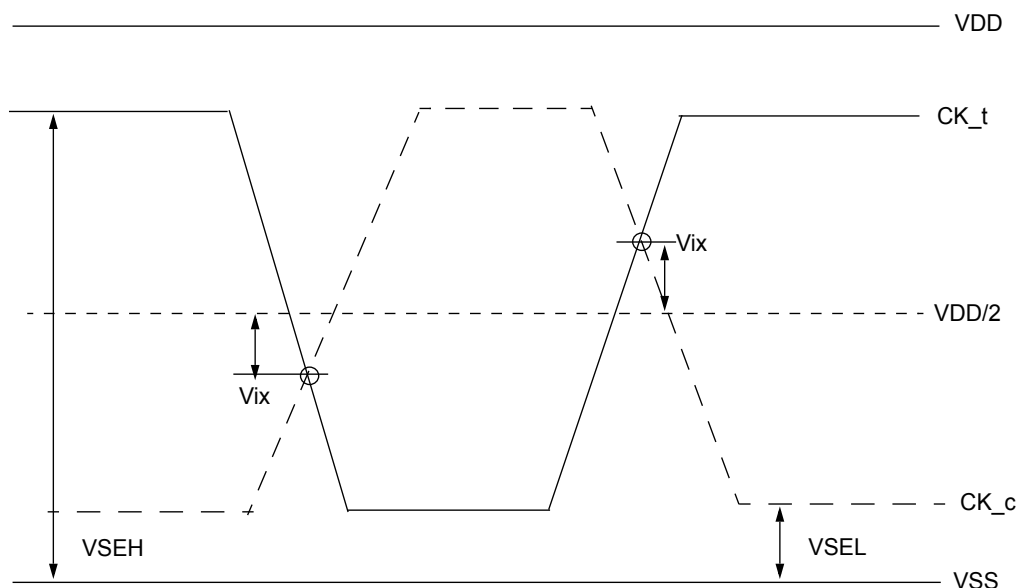


Figure 5. Vix Definition (CK)

[Table 10] Cross Point Voltage for Differential Input Signals (CK)

Symbol	Parameter	DDR4-1600/1866/2133			
		min		max	
-	Area of VSEH, VSEL	$VSEL \leq VDD/2 - 145mV$	$VDD/2 - 145mV \leq VSEL \leq VDD/2 - 100mV$	$VDD/2 + 100mV \leq VSEL \leq VDD/2 + 145mV$	$VDD/2 + 145mV \leq VSEL$
VIX(CK)	Differential Input Cross Point Voltage relative to VDD/2 for CK _t , CK _c	-120mV	$-(VDD/2 - VSEL) + 25mV$	$(VSEH - VDD/2) - 25mV$	120mV

Symbol	Parameter	DDR4-2400			
		min		max	
-	Area of VSEH, VSEL	TBD	TBD	TBD	TBD
VIX(CK)	Differential Input Cross Point Voltage relative to VDD/2 for CK _t , CK _c	TBD	TBD	TBD	TBD

11.6 Single-ended AC & DC Output Levels

[Table 11] Single-ended AC & DC Output Levels

Symbol	Parameter	DDR4-1600/1866/2133/2400	Units	NOTE
$V_{OH}(DC)$	DC output high measurement level (for IV curve linearity)	$1.1 \times V_{DDQ}$	V	
$V_{OM}(DC)$	DC output mid measurement level (for IV curve linearity)	$0.8 \times V_{DDQ}$	V	
$V_{OL}(DC)$	DC output low measurement level (for IV curve linearity)	$0.5 \times V_{DDQ}$	V	
$V_{OH}(AC)$	AC output high measurement level (for output SR)	$(0.7 + 0.15) \times V_{DDQ}$	V	1
$V_{OL}(AC)$	AC output low measurement level (for output SR)	$(0.7 - 0.15) \times V_{DDQ}$	V	1

NOTE :

1. The swing of $\pm 0.15 \times V_{DDQ}$ is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of $RZQ/7\Omega$ and an effective test load of 50Ω to $V_{TT} = V_{DDQ}$.

11.7 Differential AC & DC Output Levels

[Table 12] Differential AC & DC Output Levels

Symbol	Parameter	DDR4-1600/1866/2133/2400	Units	NOTE
$V_{OHdiff}(AC)$	AC differential output high measurement level (for output SR)	$+0.3 \times V_{DDQ}$	V	1
$V_{OLdiff}(AC)$	AC differential output low measurement level (for output SR)	$-0.3 \times V_{DDQ}$	V	1

NOTE :

1. The swing of $\pm 0.3 \times V_{DDQ}$ is based on approximately 50% of the static differential output peak-to-peak swing with a driver impedance of $RZQ/7\Omega$ and an effective test load of 50Ω to $V_{TT} = V_{DDQ}$ at each of the differential outputs.

11.8 Single-ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OL}(AC)$ and $V_{OH}(AC)$ for single ended signals as shown in Table 13 and Figure 6.

[Table 13] Single-ended Output Slew Rate Definition

Description	Measured		Defined by
	From	To	
Single ended output slew rate for rising edge	$V_{OL}(AC)$	$V_{OH}(AC)$	$[V_{OH}(AC) - V_{OL}(AC)] / \Delta TRse$
Single ended output slew rate for falling edge	$V_{OH}(AC)$	$V_{OL}(AC)$	$[V_{OH}(AC) - V_{OL}(AC)] / \Delta TFse$

NOTE :

1. Output slew rate is verified by design and characterization, and may not be subject to production test.

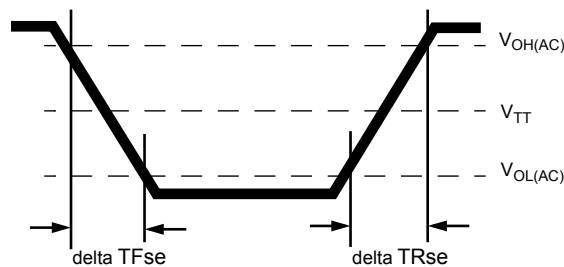


Figure 6. Single-ended Output Slew Rate Definition

[Table 14] Single-ended Output Slew Rate

Parameter	Symbol	DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Single ended output slew rate	SRQse	4	9	4	9	4	9	4	9	V/ns

Description: SR: Slew Rate

Q: Query Output (like in DQ, which stands for Data-in, Query-Output)

se: Single-ended Signals

For Ron = RZQ/7 setting

NOTE :

1. In two cases, a maximum slew rate of 12 V/ns applies for a single DQ signal within a byte lane.

-Case 1 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are static (i.e. they stay at either high or low).

-Case 2 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are switching into the opposite direction (i.e. from low to high or high to low respectively). For the remaining DQ signal switching into the opposite direction, the regular maximum limit of 9 V/ns applies

11.9 Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOLdiff(AC) and VOHdiff(AC) for differential signals as shown in Table 15 and Figure 7.

[Table 15] Differential Output Slew Rate Definition

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	VOLdiff(AC)	VOHdiff(AC)	$[V_{OHdiff}(AC) - V_{OLdiff}(AC)] / \Delta TR_{diff}$
Differential output slew rate for falling edge	VOHdiff(AC)	VOLdiff(AC)	$[V_{OHdiff}(AC) - V_{OLdiff}(AC)] / \Delta TF_{diff}$

NOTE:

1. Output slew rate is verified by design and characterization, and may not be subject to production test.

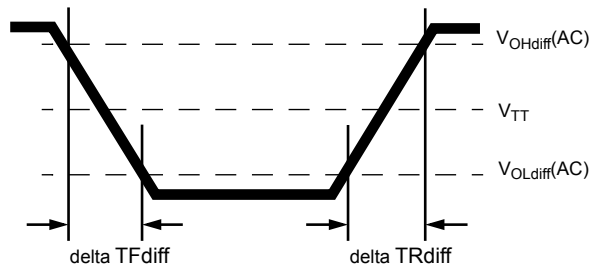


Figure 7. Differential Output Slew Rate Definition

[Table 16] Differential Output Slew Rate

Parameter	Symbol	DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Differential output slew rate	SRQdiff	8	18	8	18	8	18	8	18	V/ns

Description:

SR: Slew Rate

Q: Query Output (like in DQ, which stands for Data-in, Query-Output)

diff: Differential Signals

For Ron = RZQ/7 setting

11.10 Single-ended AC & DC Output Levels of Connectivity Test Mode

Following output parameters will be applied for DDR4 SDRAM Output Signal during Connectivity Test Mode.

[Table 17] Single-ended AC & DC Output Levels of Connectivity Test Mode

Symbol	Parameter	DDR4-1600/1866/2133/2400	Unit	Notes
$V_{OH(DC)}$	DC output high measurement level (for IV curve linearity)	$1.1 \times V_{DDQ}$	V	
$V_{OM(DC)}$	DC output mid measurement level (for IV curve linearity)	$0.8 \times V_{DDQ}$	V	
$V_{OL(DC)}$	DC output low measurement level (for IV curve linearity)	$0.5 \times V_{DDQ}$	V	
$V_{OB(DC)}$	DC output below measurement level (for IV curve linearity)	$0.2 \times V_{DDQ}$	V	
$V_{OH(AC)}$	AC output high measurement level (for output SR)	$V_{TT} + (0.1 \times V_{DDQ})$	V	1
$V_{OL(AC)}$	AC output below measurement level (for output SR)	$V_{TT} - (0.1 \times V_{DDQ})$	V	1

NOTE:

1. The effective test load is 50Ω terminated by $V_{TT} = 0.5 \times V_{DDQ}$.

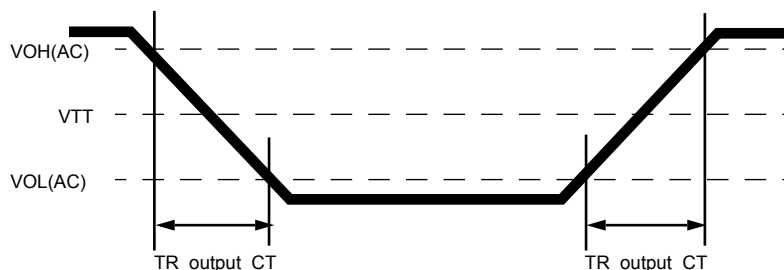


Figure 8. Output Slew Rate Definition of Connectivity Test Mode

[Table 18] Single-ended Output Slew Rate of Connectivity Test Mode

Parameter	Symbol	DDR4-1600/1866/2133/2400		Unit	Notes
		Min	Max		
Output signal Falling time	TF_output_CT	-	10	ns/V	
Output signal Rising time	TR_output_CT	-	10	ns/V	

11.11 Test Load for Connectivity Test Mode Timing

The reference load for ODT timings is defined in Figure 9.

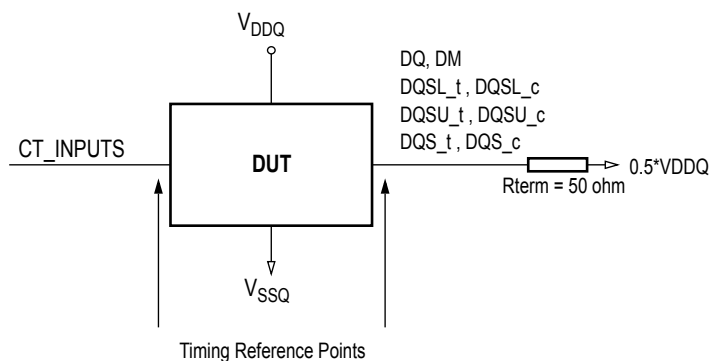


Figure 9. Connectivity Test Mode Timing Reference Load

12. DIMM IDD Specification Definition

[Table 19] Basic IDD, IPP and IDDQ Measurement Conditions

Symbol	Description
IDD0	Operating One Bank Active-Precharge Current (AL=0) CKE: High; External clock: On; tCK, nRC, nRAS, CL: Refer to Component Datasheet for detail pattern; BL: 8 ¹ ; AL: 0; CS_n: High between ACT and PRE; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,...; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern
IDD0A	Operating One Bank Active-Precharge Current (AL=CL-1) AL = CL-1, Other conditions: see IDD0
IPP0	Operating One Bank Active-Precharge IPP Current Same condition with IDD0
IDD1	Operating One Bank Active-Read-Precharge Current (AL=0) CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: Refer to Component Datasheet for detail pattern; BL: 8 ¹ ; AL: 0; CS_n: High between ACT, RD and PRE; Command, Address, Bank Group Address, Bank Address Inputs, Data IO: partially toggling; DM_n: stable at 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,...; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern
IDD1A	Operating One Bank Active-Read-Precharge Current (AL=CL-1) AL = CL-1, Other conditions: see IDD1
IPP1	Operating One Bank Active-Read-Precharge IPP Current Same condition with IDD1
IDD2N	Precharge Standby Current (AL=0) CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 8 ¹ ; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern
IDD2NA	Precharge Standby Current (AL=CL-1) AL = CL-1, Other conditions: see IDD2N
IPP2N	Precharge Standby IPP Current Same condition with IDD2N
IDD2NT	Precharge Standby ODT Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 8 ¹ ; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling; Data IO: VSSQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: toggling according; Pattern Details: Refer to Component Datasheet for detail pattern
IDDQ2NT (Optional)	Precharge Standby ODT IDDQ Current Same definition like for IDD2NT, however measuring IDDQ current instead of IDD current
IDD2NL	Precharge Standby Current with CAL enabled Same definition like for IDD2N, CAL enabled³
IDD2NG	Precharge Standby Current with Gear Down mode enabled Same definition like for IDD2N, Gear Down mode enabled^{3,5}
IDD2ND	Precharge Standby Current with DLL disabled Same definition like for IDD2N, DLL disabled³
IDD2N_par	Precharge Standby Current with CA parity enabled Same definition like for IDD2N, CA parity enabled³
IDD2P	Precharge Power-Down Current CKE: Low; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 8 ¹ ; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: stable at 0
IPP2P	Precharge Power-Down IPP Current Same condition with IDD2P
IDD2Q	Precharge Quiet Standby Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 8 ¹ ; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: stable at 0

Symbol	Description
IDD3N	Active Standby Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 8 ¹ ; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern
IDD3NA	Active Standby Current (AL=CL-1) AL = CL-1, Other conditions: see IDD3N
IPP3N	Active Standby IPP Current Same condition with IDD3N
IDD3P	Active Power-Down Current CKE: Low; External clock: On; tCK, CL: sRefer to Component Datasheet for detail pattern; BL: 8 ¹ ; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: stable at 0
IPP3P	Active Power-Down IPP Current Same condition with IDD3P
IDD4R	Operating Burst Read Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 8 ² ; AL: 0; CS_n: High between RD; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling; Data IO: seamless read data burst with different data between one burst and the next one according; DM_n: stable at 1; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,...; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern
IDD4RA	Operating Burst Read Current (AL=CL-1) AL = CL-1, Other conditions: see IDD4R
IDD4RB	Operating Burst Read Current with Read DBI Read DBI enabled ³ , Other conditions: see IDD4R
IPP4R	Operating Burst Read IPP Current Same condition with IDD4R
IDDQ4R (Optional)	Operating Burst Read IDDQ Current Same definition like for IDD4R, however measuring IDDQ current instead of IDD current
IDDQ4RB (Optional)	Operating Burst Read IDDQ Current with Read DBI Same definition like for IDD4RB, however measuring IDDQ current instead of IDD current
IDD4W	Operating Burst Write Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 8 ¹ ; AL: 0; CS_n: High between WR; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling; Data IO: seamless write data burst with different data between one burst and the next one; DM_n: stable at 1; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,...; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: stable at HIGH; Pattern Details: Refer to Component Datasheet for detail pattern
IDD4WA	Operating Burst Write Current (AL=CL-1) AL = CL-1, Other conditions: see IDD4W
IDD4WB	Operating Burst Write Current with Write DBI Write DBI enabled ³ , Other conditions: see IDD4W
IDD4WC	Operating Burst Write Current with Write CRC Write CRC enabled ³ , Other conditions: see IDD4W
IDD4W_par	Operating Burst Write Current with CA Parity CA Parity enabled ³ , Other conditions: see IDD4W
IPP4W	Operating Burst Write IPP Current Same condition with IDD4W
IDD5B	Burst Refresh Current (1X REF) CKE: High; External clock: On; tCK, CL, nRFC: Refer to Component Datasheet for detail pattern; BL: 8 ¹ ; AL: 0; CS_n: High between REF; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: REF command every nRFC; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern
IPP5B	Burst Refresh Write IPP Current (1X REF) Same condition with IDD5B
IDD5F2	Burst Refresh Current (2X REF) tRFC=tRFC_x2, Other conditions: see IDD5B
IPP5F2	Burst Refresh Write IPP Current (2X REF) Same condition with IDD5F2

Symbol	Description
IDD5F4	Burst Refresh Current (4X REF) tRFC=tRFC_x4, Other conditions: see IDD5B
IPP5F4	Burst Refresh Write IPP Current (4X REF) Same condition with IDD5F4
IDD6N	Self Refresh Current: Normal Temperature Range T_{CASE}: 0 - 85°C; Low Power Array Self Refresh (LP ASR) : Normal ⁴ ; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 8 ¹ ; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n: stable at 1; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: MID-LEVEL
IPP6N	Self Refresh IPP Current: Normal Temperature Range Same condition with IDD6N
IDD6E	Self-Refresh Current: Extended Temperature Range¹ T_{CASE}: 0 - 95°C; Low Power Array Self Refresh (LP ASR) : Extended ⁴ ; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 8 ¹ ; AL: 0; CS_n, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n: stable at 1; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: MID-LEVEL
IPP6E	Self Refresh IPP Current: Extended Temperature Range Same condition with IDD6E
IDD6R	Self-Refresh Current: Reduced Temperature Range T_{CASE}: 0 - 45°C; Low Power Array Self Refresh (LP ASR) : Reduced ⁴ ; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 8 ¹ ; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n: stable at 1; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: MID-LEVEL
IPP6R	Self Refresh IPP Current: Reduced Temperature Range Same condition with IDD6R
IDD6A	Auto Self-Refresh Current T_{CASE}: 0 - 95°C; Low Power Array Self Refresh (LP ASR) : Auto ⁴ ; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 8 ¹ ; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n: stable at 1; Bank Activity: Auto Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: MID-LEVEL
IPP6A	Auto Self-Refresh IPP Current Same condition with IDD6A
IDD7	Operating Bank Interleave Read Current CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL: Refer to Component Datasheet for detail pattern; BL: 8 ¹ ; AL: CL-1; CS_n: High between ACT and RDA; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: read data bursts with different data between one burst and the next one ; DM_n: stable at 1; Bank Activity: two times interleaved cycling through banks (0, 1, ...7) with different addressing; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern
IPP7	Operating Bank Interleave Read IPP Current Same condition with IDD7
IDD8	Maximum Power Down Current TBD
IPP8	Maximum Power Down IPP Current Same condition with IDD8

NOTE :

1. Burst Length: BL8 fixed by MRS: set MR0 [A1:0=00]
2. Output Buffer Enable
 - set MR1 [A12 = 0] : Qoff = Output buffer enabled
 - set MR1 [A2:1 = 00] : Output Driver Impedance Control = RZQ/7
- RTT_Nom enable
 - set MR1 [A10:8 = 011] : RTT_NOM = RZQ/6
- RTT_WR enable
 - set MR2 [A10:9 = 01] : RTT_WR = RZQ/2
- RTT_PARK disable
 - set MR5 [A8:6 = 000]
3. CAL enabled : set MR4 [A8:6 = 001] : 1600MT/s
010] : 1866MT/s, 2133MT/s
011] : 2400MT/s
- Gear Down mode enabled :set MR3 [A3 = 1] : 1/4 Rate
- DLL disabled : set MR1 [A0 = 0]
- CA parity enabled :set MR5 [A2:0 = 001] : 1600MT/s, 1866MT/s, 2133MT/s
010] : 2400MT/s
- Read DBI enabled : set MR5 [A12 = 1]
- Write DBI enabled : set :MR5 [A11 = 1]
4. Low Power Auto Self Refresh (LP ASR) : set MR2 [A7:6 = 00] : Normal
01] : Reduced Temperature range
10] : Extended Temperature range
11] : Auto Self Refresh
5. IDD2NG should be measured after sync pules(NOP) input.

13. IDD SPEC Table

IDD and IPP values are for typical operating range of voltage and temperature unless otherwise noted.

[Table 20] I_{DD} and I_{DDQ} Specification

Symbol	M391A5143EB1 : 4GB(512Mx72) Module				Unit	NOTE
	DDR4-2133		DDR4-2400			
	15-15-15		17-17-17			
	VDD 1.2V	VPP 2.5V	VDD 1.2V	VPP 2.5V		
	IDD Max.	IPP Max.	IDD Max.	IPP Max.		
I _{DD0}	270	36	279	36	mA	
I _{DD0A}	288	36	297	36	mA	
I _{DD1}	360	27	378	27	mA	
I _{DD1A}	387	27	405	27	mA	
I _{DD2N}	135	27	135	27	mA	
I _{DD2NA}	162	27	171	27	mA	
I _{DD2NT}	144	27	153	27	mA	
I _{DD2NL}	99	27	108	27	mA	
I _{DD2NG}	135	27	144	27	mA	
I _{DD2ND}	108	27	108	27	mA	
I _{DD2N_par}	135	27	135	27	mA	
I _{DD2P}	90	27	90	27	mA	
I _{DD2Q}	117	27	117	27	mA	
I _{DD3N}	243	27	252	27	mA	
I _{DD3NA}	252	27	261	27	mA	
I _{DD3P}	117	27	117	27	mA	
I _{DD4R}	756	27	810	27	mA	
I _{DD4RA}	783	27	855	27	mA	
I _{DD4RB}	783	27	846	27	mA	
I _{DD4W}	648	27	702	27	mA	
I _{DD4WA}	684	27	729	27	mA	
I _{DD4WB}	648	27	693	27	mA	
I _{DD4WC}	594	27	630	27	mA	
I _{DD4W_par}	702	27	765	27	mA	
I _{DD5B}	1710	162	1728	162	mA	
I _{DD5F2}	1440	135	1458	135	mA	
I _{DD5F4}	1080	99	1098	99	mA	
I _{DD6N}	117	36	117	36	mA	
I _{DD6E}	180	36	180	45	mA	
I _{DD6R}	90	36	90	31.5	mA	
I _{DD6A}	117	36	117	36	mA	
I _{DD7}	1314	81	1332	81	mA	
I _{DD8}	59	18	59	18	mA	

NOTE :

- DIMM IDD SPEC is based on the condition that de-activated rank(IDLE) is IDD2N. Please refer to Table21.
- IDD current measure method and detail patterns are described on DDR4 component datasheet.
- VDD and VDDQ are merged on module PCB (IDDQ values are not considered by Qoff condition)
- DIMM IDD Values are calculated based on the component IDD spec and Register power.

Symbol	M391A1G43EB1 : 8GB(1Gx72) Module				Unit	NOTE
	DDR4-2133		DDR4-2400			
	15-15-15		17-17-17			
	VDD 1.2V	VPP 2.5V	VDD 1.2V	VPP 2.5V		
	IDD Max.	IPP Max.	IDD Max.	IPP Max.		
I _{DD0}	405	63	414	63	mA	
I _{DD0A}	423	63	432	63	mA	
I _{DD1}	495	54	513	54	mA	
I _{DD1A}	522	54	540	54	mA	
I _{DD2N}	270	54	270	54	mA	
I _{DD2NA}	324	54	342	54	mA	
I _{DD2NT}	288	54	306	54	mA	
I _{DD2NL}	198	54	216	54	mA	
I _{DD2NG}	270	54	288	54	mA	
I _{DD2ND}	216	54	216	54	mA	
I _{DD2N_par}	270	54	270	54	mA	
I _{DD2P}	180	54	180	54	mA	
I _{DD2Q}	234	54	234	54	mA	
I _{DD3N}	486	54	504	54	mA	
I _{DD3NA}	504	54	522	54	mA	
I _{DD3P}	234	54	234	54	mA	
I _{DD4R}	891	54	945	54	mA	
I _{DD4RA}	918	54	990	54	mA	
I _{DD4RB}	918	54	981	54	mA	
I _{DD4W}	783	54	837	54	mA	
I _{DD4WA}	819	54	864	54	mA	
I _{DD4WB}	783	54	828	54	mA	
I _{DD4WC}	729	54	765	54	mA	
I _{DD4W_par}	837	54	900	54	mA	
I _{DD5B}	1845	189	1863	189	mA	
I _{DD5F2}	1575	162	1593	162	mA	
I _{DD5F4}	1215	126	1233	126	mA	
I _{DD6N}	234	72	234	72	mA	
I _{DD6E}	360	72	360	90	mA	
I _{DD6R}	180	72	180	63	mA	
I _{DD6A}	234	72	234	72	mA	
I _{DD7}	1449	108	1467	108	mA	
I _{DD8}	117	36	117	36	mA	

NOTE :

1. DIMM IDD SPEC is based on the condition that de-activated rank(IDLE) is IDD2N. Please refer to Table21.
2. IDD current measure method and detail patterns are described on DDR4 component datasheet.
3. VDD and VDDQ are merged on module PCB (IDDQ values are not considered by Qoff condition)
4. DIMM IDD Values are calculated based on the component IDD spec and Register power.

[Table 21] DIMM Rank Status

SEC DIMM	Operating Rank	The other Rank
<i>I</i> _{DD0}	<i>I</i> _{DD0}	<i>I</i> _{DD2N}
<i>I</i> _{DD1}	<i>I</i> _{DD1}	<i>I</i> _{DD2N}
<i>I</i> _{DD2P}	<i>I</i> _{DD2P}	<i>I</i> _{DD2P}
<i>I</i> _{DD2N}	<i>I</i> _{DD2N}	<i>I</i> _{DD2N}
<i>I</i> _{DD2Q}	<i>I</i> _{DD2Q}	<i>I</i> _{DD2Q}
<i>I</i> _{DD3P}	<i>I</i> _{DD3P}	<i>I</i> _{DD3P}
<i>I</i> _{DD3N}	<i>I</i> _{DD3N}	<i>I</i> _{DD3N}
<i>I</i> _{DD4R}	<i>I</i> _{DD4R}	<i>I</i> _{DD2N}
<i>I</i> _{DD4W}	<i>I</i> _{DD4W}	<i>I</i> _{DD2N}
<i>I</i> _{DD5B}	<i>I</i> _{DD5B}	<i>I</i> _{DD2N}
<i>I</i> _{DD6}	<i>I</i> _{DD6}	<i>I</i> _{DD6}
<i>I</i> _{DD7}	<i>I</i> _{DD7}	<i>I</i> _{DD2N}
<i>I</i> _{DD8}	<i>I</i> _{DD8}	<i>I</i> _{DD8}

14. Input/Output Capacitance

[Table 22] Silicon Pad I/O Capacitance

Symbol	Parameter	DDR4-1600/1866/2133		DDR4-2400		Unit	NOTE
		min	max	min	max		
C_{IO}	Input/output capacitance	0.55	1.4	0.55	1.15	pF	1,2,3
C_{DIO}	Input/output capacitance delta	-0.1	0.1	-0.1	0.1	pF	1,2,3,11
C_{DDQS}	Input/output capacitance delta DQS_t and DQS_c	-	0.05	-	0.05	pF	1,2,3,5
C_{CK}	Input capacitance, CK_t and CK_c	0.2	0.8	0.2	0.7	pF	1,3
C_{DCK}	Input capacitance delta CK_t and CK_c	-	0.05	-	0.05	pF	1,3,4
C_I	Input capacitance (CTRL, ADD, CMD pins only)	0.2	0.8	0.2	0.7	pF	1,3,6
C_{DI_CTRL}	Input capacitance delta (All CTRL pins only)	-0.1	0.1	-0.1	0.1	pF	1,3,7,8
$C_{DI_ADD_CMD}$	Input capacitance delta (All ADD/CMD pins only)	-0.1	0.1	-0.1	0.1	pF	1,2,9,10
C_{ALERT}	Input/output capacitance of ALERT	0.5	1.5	0.5	1.5	pF	1,3
C_{ZQ}	Input/output capacitance of ZQ	-	2.3	-	2.3	pF	1,3,12
C_{TEN}	Input capacitance of TEN	0.2	2.3	0.2	2.3	pF	1,3,13

NOTE:

1. This parameter is not subject to production test. It is verified by design and characterization. The silicon only capacitance is validated by de-embedding the package L & C parasitic. The capacitance is measured with VDD, VDDQ, VSS, VSSQ applied with all other signal pins floating. Measurement procedure tbd.
2. DQ, DM_n, DQS_T, DQS_c, TDQS_T, TDQS_C. Although the DM, TDQS_T and TDQS_C pins have different functions, the loading matches DQ and DQS
3. This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here
4. Absolute value CK_T-CK_C
5. Absolute value of CIO(DQS_T)-CIO(DQS_c)
6. CI applies to ODT, CS_n, CKE, A0-A17, BA0-BA1, BG0-BG1, RAS_n/A16, CAS_n/A15, WE_n/A14, ACT_n and PAR.
7. CDI CTRL applies to ODT, CS_n and CKE
8. $CDI_CTRL = CI(CTRL) - 0.5 * (CI(CLK_T) + CI(CLK_C))$
9. CDI_ADD_CMD applies to, A0-A17, BA0-BA1, BG0-BG1, RAS_n/A16, CAS_n/A15, WE_n/A14, ACT_n and PAR.
10. $CDI_ADD_CMD = CI(ADD_CMD) - 0.5 * (CI(CLK_T) + CI(CLK_C))$
11. $CDIO = CIO(DQ, DM) - 0.5 * (CIO(DQS_T) + CIO(DQS_c))$
12. Maximum external load capacitance on ZQ pin: tbd pF.
13. TEN pin may be DRAM internally pulled low through a weak pull-down resistor to VSS. In this case CTEN might not be valid and system shall verify TEN signal with Vendor specific information.

15. Electrical Characteristics and AC Timing

15.1 Speed Bins and CL, tRCD, tRP, tRC and tRAS for Corresponding Bin

[Table 23] DDR4-1600 Speed Bins and Operations

Speed Bin				DDR4-1600		Unit	NOTE
CL-nRCD-nRP				11-11-11			
Parameter		Symbol	min	max			
Internal read command to first data		tAA	13.75 ¹² (13.50) ^{5,10}	18.00	ns	10	
Internal read command to first data with read DBI enabled		tAA_DBI	tAA(min) + 2nCK	tAA(max) +2nCK	ns	10	
ACT to internal read or write delay time		tRCD	13.75 (13.50) ^{5,10}	-	ns	10	
PRE command period		tRP	13.75 (13.50) ^{5,10}	-	ns	10	
ACT to PRE command period		tRAS	35	9 x tREFI	ns	10	
ACT to ACT or REF command period		tRC	48.75 (48.50) ^{5,10}	-	ns	10	
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11	tCK(AVG)	1.5	1.6	ns	1,2,3,4,10,13
				(Optional) ^{5,10}		ns	
		CL = 10	CL = 12	tCK(AVG)	Reserved		ns
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3
Supported CL Settings				9,11,12		nCK	12,13
Supported CL Settings with read DBI				11,13,14		nCK	12
Supported CWL Settings				9,11		nCK	

[Table 24] DDR4-1866 Speed Bins and Operations

Speed Bin			DDR4-1866		Unit	NOTE	
CL-nRCD-nRP			13-13-13				
Parameter	Symbol	min	max				
Internal read command to first data	tAA	13.92 ¹² (13.50) ^{5,10}	18.00	ns	11		
Internal read command to first data with read DBI enabled	tAA_DBI	tAA(min) + 2nCK	tAA(max) + 2nCK	ns	11		
ACT to internal read or write delay time	tRCD	13.92 ¹² (13.50) ^{5,10}	-	ns	11		
PRE command period	tRP	13.92 ¹² (13.50) ^{5,10}	-	ns	11		
ACT to PRE command period	tRAS	34	9 x tREFI	ns	11		
ACT to ACT or REF command period	tRC	47.92 (47.50) ^{5,10}	-	ns	11		
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11	tCK(AVG)	1.5 (Optional) ^{5,10}	1.6	ns	1,2,3,4,10,12
	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	1,2,3,4,10
	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	4
CWL = 9,11	CL = 11	CL = 13	tCK(AVG)	1.25 (Optional) ^{5,10}	<1.5	ns	1,2,3,4,6
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,6
	CL = 12	CL = 14	tCK(AVG)	Reserved		ns	1,2,3,4
CWL = 10,12	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3
	Supported CL Settings			9,11,12,13,14		nCK	11,12
Supported CL Settings with read DBI			11,13,14,15,16		nCK	11	
Supported CWL Settings			9,10,11,12		nCK		

[Table 25] DDR4-2133 Speed Bins and Operations

Speed Bin			DDR4-2133		Unit	NOTE	
CL-nRCD-nRP			15-15-15				
Parameter		Symbol	min	max			
Internal read command to first data		tAA	14.06 ¹² (13.75) ^{5,10}	18.00	ns	10	
Internal read command to first data with read DBI enabled		tAA_DBI	tAA(min) + 3nCK	tAA(max) + 3nCK	ns	10	
ACT to internal read or write delay time		tRCD	14.06 ¹² (13.75) ^{5,10}	-	ns	10	
PRE command period		tRP	14.06 (13.75) ^{5,10}	-	ns	10	
ACT to PRE command period		tRAS	33	9 x tREFI	ns	10	
ACT to ACT or REF command period		tRC	47.06 (46.75) ^{5,10}	-	ns	10	
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11	tCK(AVG)	1.5 (Optional) ^{5,10}	1.6	ns	1,2,3,4,9,11 2
	CL = 10	CL = 12	tCK(AVG)	Reserved			
CWL = 9,11	CL = 11	CL = 13	tCK(AVG)	1.25 (Optional) ^{5,11}	<1.5	ns	1,2,3,4,7
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,7
CWL = 10,12	CL = 13	CL = 15	tCK(AVG)	1.071 (Optional) ^{5,10}	<1.25	ns	1,2,3,4,7
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3,7
CWL = 11,14	CL = 14	CL = 17	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 15	CL = 18	tCK(AVG)	0.937	<1.071	ns	1,2,3,4
	CL = 16	CL = 19	tCK(AVG)	0.937	<1.071	ns	1,2,3
Supported CL Settings			9,11,12,13,14,15,16		nCK	11,12	
Supported CL Settings with read DBI			11,13,14,15,16,18,19		nCK		
Supported CWL Settings			9,10,11,12,14		nCK		

[Table 26] DDR4-2400 Speed Bins and Operations

Speed Bin			DDR4-2400		Unit	NOTE	
CL-nRCD-nRP			17-17-17				
Parameter		Symbol	min	max			
Internal read command to first data		tAA	14.16 (13.75) ^{5,10}	18.00	ns	10	
Internal read command to first data with read DBI enabled		tAA_DBI	tAA(min) + 3nCK	tAA(max) + 3nCK	ns	10	
ACT to internal read or write delay time		tRCD	14.16 (13.75) ^{5,10}	-	ns	10	
PRE command period		tRP	14.16 (13.75) ^{5,10}	-	ns	10	
ACT to PRE command period		tRAS	32	9 x tREFI	ns	10	
ACT to ACT or REF command period		tRC	46.16 (45.75) ^{5,10}	-	ns	10	
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11	tCK(AVG)	Reserved		ns	1,2,3,4,9
	CL = 10	CL = 12	tCK(AVG)	1.5	1.6	ns	1,2,3,4,9
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	4
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4,8
				(Optional) ^{5,10}			
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,8
CWL = 10,12	CL = 12	CL = 14	tCK(AVG)	Reserved		ns	4
	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4,8
				(Optional) ^{5,10}			
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3,8
CWL = 11,14	CL = 14	CL = 17	tCK(AVG)	Reserved		ns	4
	CL = 15	CL = 18	tCK(AVG)	0.937	<1.071	ns	1,2,3,4,8
				(Optional) ^{5,10}			
	CL = 16	CL = 19	tCK(AVG)	0.937	<1.071	ns	1,2,3,8
CWL = 12,16	CL = 15	CL = 18	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 16	CL = 19	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 17	CL = 20	tCK(AVG)	0.833	<0.937		
	CL = 18	CL = 21	tCK(AVG)	0.833	<0.937	ns	1,2,3
Supported CL Settings			10,11,12,13,14,15,16,17,18		nCK	12	
Supported CL Settings with read DBI			12,13,14,15,16,18,19,20,21		nCK		
Supported CWL Settings			9,10,11,12,14,16		nCK		

15.2 Speed Bin Table Note

Absolute Specification

- VDDQ = VDD = 1.20V +/- 0.06 V
- VPP = 2.5V +0.25/-0.125 V
- The values defined with above-mentioned table are DLL ON case.
- DDR4-1600, 1866, 2133, 2400 Speed Bin Tables are valid only when Geardown Mode is disabled.

1. The CL setting and CWL setting result in tCK(avg).MIN and tCK(avg).MAX requirements. When making a selection of tCK(avg), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. tCK(avg).MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. CL in clock cycle is calculated from tAA following rounding algorithm defined in Section "Rounding Algorithms".
3. tCK(avg).MAX limits: Calculate tCK(avg) = tAA.MAX / CL SELECTED and round the resulting tCK(avg) down to the next valid speed bin (i.e. 1.5ns or 1.25ns or 1.071 ns or 0.937 ns or 0.833 ns). This result is tCK(avg).MAX corresponding to CL SELECTED.
4. 'Reserved' settings are not allowed. User must program a different value.
5. 'Optional' settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature. Refer to supplier's data sheet and/or the DIMM SPD information if and how this setting is supported.
6. Any DDR4-1866 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
7. Any DDR4-2133 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
8. Any DDR4-2400 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
9. DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate.
10. Parameters apply from tCK(avg)min to tCK(avg)max at all standard JEDEC clock period values as stated in the Speed Bin Tables.
11. CL number in parentheses, it means that these numbers are optional.
12. DDR4 SDRAM supports CL=9 as long as a system meets tAA(min).
13. Each speed bin lists the timing requirements that need to be supported in order for a given DRAM to be JEDEC compliant. JEDEC compliance does not require support for all speed bins within a given speed. JEDEC compliance requires meeting the parameters for a least one of the listed speed bins.

16. Timing Parameters by Speed Grade

[Table 27] Timing Parameters by Speed Bin for DDR4-1600 to DDR4-2400

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Units	NOTE	
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX			
Clock Timing												
Minimum Clock Cycle Time (DLL off mode)	tCK (DLL_OFF)	8	20	8	20	8	20	8	20	ns		
Average Clock Period	tCK(avg)	1.25	<1.5	1.071	<1.25	0.937	<1.071	0.833	<0.937	ns	35,36	
Average high pulse width	tCH(avg)	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)		
Average low pulse width	tCL(avg)	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)		
Absolute Clock Period	tCK(abs)	tCK(avg)min + tJIT(per)min_tot tCK(avg)max + tJIT(per)max_tot									tCK(avg)	
Absolute clock HIGH pulse width	tCH(abs)	0.45	-	0.45	-	0.45	-	0.45	-	tCK(avg)	23	
Absolute clock LOW pulse width	tCL(abs)	0.45	-	0.45	-	0.45	-	0.45	-	tCK(avg)	24	
Clock Period Jitter- total	JIT(per)_tot	-63	63	-54	54	-47	47	-42	42	ps	23	
Clock Period Jitter- deterministic	JIT(per)_dj	-31	31	-27	27	-23	23	-21	21	ps	26	
Clock Period Jitter during DLL locking period	tJIT(per, lck)	-50	50	-43	43	-38	38	-33	33	ps		
Cycle to Cycle Period Jitter	tJIT(cc)	-	125	-	107	-	94	-	83	ps		
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	-	100	-	86	-	75	-	67	ps		
Duty Cycle Jitter	tJIT(duty)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ps		
Cumulative error across 2 cycles	tERR(2per)	-92	92	-79	79	-69	69	-61	61	ps		
Cumulative error across 3 cycles	tERR(3per)	-109	109	-94	94	-82	82	-73	73	ps		
Cumulative error across 4 cycles	tERR(4per)	-121	121	-104	104	-91	91	-81	81	ps		
Cumulative error across 5 cycles	tERR(5per)	-131	131	-112	112	-98	98	-87	87	ps		
Cumulative error across 6 cycles	tERR(6per)	-139	139	-119	119	-104	104	-92	92	ps		
Cumulative error across 7 cycles	tERR(7per)	-145	145	-124	124	-109	109	-97	97	ps		
Cumulative error across 8 cycles	tERR(8per)	-151	151	-129	129	-113	113	-101	101	ps		
Cumulative error across 9 cycles	tERR(9per)	-156	156	-134	134	-117	117	-104	104	ps		
Cumulative error across 10 cycles	tERR(10per)	-160	160	-137	137	-120	120	-107	107	ps		
Cumulative error across 11 cycles	tERR(11per)	-164	164	-141	141	-123	123	-110	110	ps		
Cumulative error across 12 cycles	tERR(12per)	-168	168	-144	144	-126	126	-112	112	ps		
Cumulative error across 13 cycles	tERR(13per)	-172	172	-147	147	-129	129	-114	114	ps		
Cumulative error across 14 cycles	tERR(14per)	-175	175	-150	150	-131	131	-116	116	ps		
Cumulative error across 15 cycles	tERR(15per)	-178	178	-152	152	-133	133	-118	118	ps		
Cumulative error across 16 cycles	tERR(16per)	-180	189	-155	155	-135	135	-120	120	ps		
Cumulative error across 17 cycles	tERR(17per)	-183	183	-157	157	-137	137	-122	122	ps		
Cumulative error across 18 cycles	tERR(18per)	-185	185	-159	159	-139	139	-124	124	ps		
Cumulative error across n = 13, 14 . . . 49, 50 cycles	tERR(nper)	tERR(nper)min = ((1 + 0.68ln(n)) * tJIT(per)_total min) tERR(nper)max = ((1 + 0.68ln(n)) * tJIT(per)_total max)									ps	
Command and Address setup time to CK_t, CK_c referenced to Vih(ac) / Vil(ac) levels	tIS(base)	115	-	100	-	80	-	62	-	ps		
Command and Address setup time to CK_t, CK_c referenced to Vref levels	tIS(Vref)	215	-	200	-	180	-	162	-	ps		
Command and Address hold time to CK_t, CK_c referenced to Vih(dc) / Vil(dc) levels	tIH(base)	140	-	125	-	105	-	87	-	ps		
Command and Address hold time to CK_t, CK_c referenced to Vref levels	tIH(Vref)	215	-	200	-	180	-	162	-	ps		
Control and Address Input pulse width for each input	tIPW	600	-	525	-	460	-	410	-	ps		
Command and Address Timing												
CAS_n to CAS_n command delay for same bank group	tCCD_L	max(5 nCK, 6.250 ns)	-	max(5 nCK, 5.355 ns)	-	max(5 nCK, 5.625 ns)	-	max(5 nCK, 5 ns)	-	nCK	34	
CAS_n to CAS_n command delay for different bank group	tCCD_S	4	-	4	-	4	-	4	-	nCK	34	
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(2K)	Max(4nCK,6 ns)	-	Max(4nCK,5.3ns)	-	Max(4nCK,5.3ns)	-	Max(4nCK,5.3ns)	-	nCK	34	
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(1K)	Max(4nCK,5 ns)	-	Max(4nCK,4.2ns)	-	Max(4nCK,3.7ns)	-	Max(4nCK,3.3ns)	-	nCK	34	

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
ACTIVATE to ACTIVATE Command delay to different bank group for 1/2KB page size	tRRD_S(1/2K)	Max(4nCK, 5 ns)		Max(4nCK, 4 .2ns)		Max(4nCK, 3 .7ns)		Max(4nCK, 3 .3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	tRRD_L(2K)	Max(4nCK, 7 .5ns)		Max(4nCK, 6 .4ns)		Max(4nCK, 6 .4ns)		Max(4nCK, 6 .4ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	tRRD_L(1K)	Max(4nCK, 6 ns)		Max(4nCK, 5 .3ns)		Max(4nCK, 5 .3ns)		Max(4nCK, 4 .9ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 1/2KB page size	tRRD_L(1/2K)	Max(4nCK, 6 ns)		Max(4nCK, 5 .3ns)		Max(4nCK, 5 .3ns)		Max(4nCK, 4 .9ns)	-	nCK	34
Four activate window for 2KB page size	tFAW_2K	Max(28nCK, 35ns)		Max(28nCK, 30ns)		Max(28nCK, 30ns)		Max(28nCK, 30ns)	-	ns	34
Four activate window for 1KB page size	tFAW_1K	Max(20nCK, 25ns)		Max(20nCK, 23ns)		Max(20nCK, 21ns)		Max(20nCK, 21ns)	-	ns	34
Four activate window for 1/2KB page size	tFAW_1/2K	Max(16nCK, 20ns)		Max(16nCK, 17ns)		Max(16nCK, 15ns)		Max(16nCK, 13ns)	-	ns	34
Delay from start of internal write transaction to internal read command for different bank group	tWTR_S	max(2nCK, 2 .5ns)	-	max(2nCK, 2 .5ns)	-	max(2nCK, 2 .5ns)	-	max (2nCK, 2.5ns)	-		1,2,e,3 4
Delay from start of internal write transaction to internal read command for same bank group	tWTR_L	max(4nCK, 7 .5ns)	-	max(4nCK, 7 .5ns)	-	max(4nCK, 7 .5ns)	-	max (4nCK, 7.5ns)	-		1,34
Internal READ Command to PRECHARGE Command delay	tRTP	max(4nCK, 7 .5ns)	-	max(4nCK, 7 .5ns)	-	max(4nCK, 7 .5ns)	-	max (4nCK, 7.5ns)	-		
WRITE recovery time	tWR	15	-	15	-	15	-	15	-	ns	1
Write recovery time when CRC and DM are enabled	tWR_CRC_DM	tWR+max (4nCK, 3.75n s)	-	tWR+max (5nCK, 3.75n s)	-	tWR+max (5nCK, 3.75n s)	-	tWR+max (5nCK, 3.75n s)	-	ns	1, 28
delay from start of internal write transaction to internal read command for different bank group with both CRC and DM enabled	tWTR_S_C RC_DM	tWTR_S+ma x (4nCK, 3.75n s)	-	tWTR_S+ma x (5nCK, 3.75n s)	-	tWTR_S+ma x (5nCK, 3.75n s)	-	tWTR_S+ma x (5nCK, 3.75n s)	-	ns	2, 29, 34
delay from start of internal write transaction to internal read command for same bank group with both CRC and DM enabled	tWTR_L_C RC_DM	tWTR_L+ma x (4nCK, 3.75n s)	-	tWTR_L+ma x (5nCK, 3.75n s)	-	tWTR_L+ma x (5nCK, 3.75n s)	-	tWTR_L+ma x (5nCK, 3.75n s)	-	ns	3,30, 34
DLL locking time	tDLLK	597	-	597	-	768	-	768	-	nCK	
Mode Register Set command cycle time	tMRD	8	-	8	-	8	-	8	-	nCK	
Mode Register Set command update delay	tMOD	max(24nCK, 15ns)	-	max(24nCK, 15ns)	-	max(24nCK, 15ns)	-	max(24nCK, 15ns)	-		50
Multi-Purpose Register Recovery Time	tMPRR	1	-	1	-	1	-	1	-	nCK	33
Multi Purpose Register Write Recovery Time	tWR_MPR	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-		
Auto precharge write recovery + precharge time	tDAL(min)	Programmed WR + roundup (tRP / tCK(avg))								nCK	
DQ0 or DQL0 driven to 0 set-up time to first DQS rising edge	tPDA_S	0.5	-	0.5	-	0.5	-	0.5	-	UI	45,47
DQ0 or DQL0 driven to 0 hold time from last DQS fall-ing edge	tPDA_H	0.5	-	0.5	-	0.5	-	0.5	-	UI	46,47
CS_n to Command Address Latency											
CS_n to Command Address Latency	tCAL	max(3 nCK, 3.748 ns)	-	max(3 nCK, 3.748 ns)	-	max(3 nCK, 3.748 ns)	-	5	-	nCK	
Mode Register Se commandt cycle time in CAL mode	tMRD_tCAL	tMOD+tCAL	-	tMOD+tCAL	-	tMOD+tCAL		tMOD+tCAL	-	nCK	
Mode Register Set update delay in CAL mode	tMOD_tCAL	tMOD+tCAL	-	tMOD+tCAL	-	tMOD+tCAL		tMOD+tCAL	-	nCK	
DRAM Data Timing											
DQS_t,DQS_c to DQ skew, per group, per access	tDQSQ	-	0.16	-	0.16	-	0.16	-	0.16	tCK(avg)/ 2	13,18,3 9,49
DQ output hold per group, per access from DQS_t,DQS_c	tQH	0.76	-	0.76	-	0.76	-	0.74	-	tCK(avg)/ 2	13,17,1 8,39,49
Data Valid Window per device: (tQH - tD-QSQ) of each UI on a given DRAM	tDVWd	0.63	-	0.63	-	0.64	-	0.64	-	UI	17,18,3 9,49
Data Valid Window per pin per UI: (tQH - tDQSQ) each UI on a pin of a given DRAM	tDVWp	0.66	-	0.66	-	0.69	-	0.72	-	UI	17,18,3 9,49
DQ low impedance time from CK_t, CK_c	tLZ(DQ)	-450	225	-390	195	-390	180	-330	175	ps	39
DQ high impedance time from CK_t, CK_c	tHZ(DQ)	-	225	-	195	-	180	-	175	ps	39
Data Strobe Timing											
DQS_t, DQS_c differential READ Pre-ample (1 clock preamble)	tRPRE	0.9	NOTE44	0.9	NOTE44	0.9	NOTE44	0.9	NOTE 44	tCK	39,40

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
DQS_t, DQS_c differential READ Pre-amble (2 clock preamble)	tRPRE2	NA	NA	NA	NA	NA	NA	1.8	NOTE 44	tCK	39,41
DQS_t, DQS_c differential READ Postamble	tRPST	0.33	NOTE 45	0.33	NOTE 45	0.33	NOTE 45	0.33	NOTE 45	tCK	39
DQS_t,DQS_c differential output high time	tQSH	0.4	-	0.4	-	0.4	-	0.4	-	tCK	21,39
DQS_t,DQS_c differential output low time	tQSL	0.4	-	0.4	-	0.4	-	0.4	-	tCK	20,39
DQS_t, DQS_c differential WRITE Pre-amble (1 clock preamble)	tWPRE	0.9	-	0.9	-	0.9	-	0.9	-	tCK	42
DQS_t, DQS_c differential WRITE Pre-amble (2 clock preamble)	tWPRE2	NA	-	NA	-	NA	-	1.8	-	tCK	43
DQS_t, DQS_c differential WRITE Postamble	tWPST	0.33	-	0.33	-	0.33	-	0.33	-	tCK	
DQS_t and DQS_c low-impedance time (Referenced from RL-1)	tLZ(DQS)	-450	225	-390	195	-360	180	-330	175	ps	39
DQS_t and DQS_c high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	225	-	195	-	180	-	175	ps	39
DQS_t, DQS_c differential input low pulse width	tDQSL	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tCK	
DQS_t, DQS_c differential input high pulse width	tDQSH	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tCK	
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (1 clock preamble)	tDQSS	-0.27	0.27	-0.27	0.27	-0.27	0.27	-0.27	0.27	tCK	42
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (2 clock preamble)	tDQSS2	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	tCK	43
DQS_t, DQS_c falling edge setup time to CK_t, CK_c rising edge	tDSS	0.18	-	0.18	-	0.18	-	0.18	-	tCK	
DQS_t, DQS_c falling edge hold time from CK_t, CK_c rising edge	tDSH	0.18	-	0.18	-	0.18	-	0.18	-	tCK	
DQS_t, DQS_c rising edge output timing locatino from rising CK_t, CK_c with DLL On mode	tDQSK (DLL On)	-225	225	-195	195	-180	180	-175	175	ps	37,38,39
DQS_t, DQS_c rising edge output variance window per DRAM	tDQSKI (DLL On)		370		330		310		290	ps	37,38,39
MPSM Timing											
Command path disable delay upon MPSM entry	tMPED	tMOD(min) + tCP-DED(min)	-	tMOD(min) + tCP-DED(min)	-	tMOD(min) + tCP-DED(min)	-	tMOD(min) + tCP-DED(min)	-		
Valid clock requirement after MPSM entry	tCKMPE	tMOD(min) + tCP-DED(min)	-	tMOD(min) + tCP-DED(min)	-	tMOD(min) + tCP-DED(min)	-	tMOD(min) + tCP-DED(min)	-		
Valid clock requirement before MPSM exit	tCKMPX	tCKSRX(min)	-	tCKSRX(min)	-	tCKSRX(min)	-	tCKSRX(min)	-		
Exit MPSM to commands not requiring a locked DLL	tXMP	tXS(min)	-	tXS(min)	-	tXS(min)	-	tXS(min)	-		
Exit MPSM to commands requiring a locked DLL	tXMPDLL	tXMP(min) + tXSDLL(min)	-	tXMP(min) + tXSDLL(min)	-	tXMP(min) + tXSDLL(min)	-	tXMP(min) + tXSDLL(min)	-		
CS setup time to CKE	tMPX_S	tIS(min) + tIHL(min)	-	tIS(min) + tIHL(min)	-	tIS(min) + tIHL(min)	-	tIS(min) + tIHL(min)	-		
Calibration Timing											
Power-up and RESET calibration time	tZQinit	1024	-	1024	-	1024	-	1024	-	nCK	
Normal operation Full calibration time	tZQoper	512	-	512	-	512	-	512	-	nCK	
Normal operation Short calibration time	tZQCS	128	-	128	-	128	-	128	-	nCK	
Reset/Self Refresh Timing											
Exit Reset from CKE HIGH to a valid command	tXPR	max (5nCK, tRFC(min)+10ns)	-	max (5nCK, tRFC(min)+10ns)	-	max (5nCK, tRFC(min)+10ns)	-	max (5nCK, tRFC(min)+10ns)	-	nCK	
Exit Self Refresh to commands not requiring a locked DLL	tXS	tRFC(min)+10ns	-	tRFC(min)+10ns	-	tRFC(min)+10ns	-	tRFC(min)+10ns	-	nCK	
SRX to commands not requiring a locked DLL in Self Refresh ABORT	tX-S_ABORT(min)	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	nCK	
Exit Self Refresh to ZQCL, ZQCS and MRS (CL,CWL,WR,RTP and Gear Down)	tXS_FAST(min)	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	nCK	
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	nCK	
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	tCKE(min)+1nCK	-	tCKE(min)+1nCK	-	tCKE(min)+1nCK	-	tCKE(min)+1nCK	-	nCK	
Minimum CKE low width for Self refresh entry to exit timing with CA Parity enabled	tCKESR_PAR	tCKE(min)+1nCK+PL	-	tCKE(min)+1nCK+PL	-	tCKE(min)+1nCK+PL	-	tCKE(min)+1nCK+PL	-	nCK	

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	max(5nCK, 1 0ns)	-	max(5nCK, 1 0ns)	-	max(5nCK, 1 0ns)	-	max (5nCK, 10ns)	-	nCK	
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down when CA Parity is enabled	tCKSRE_PAR	max (5nCK, 10ns) +PL	-	max (5nCK, 10ns) +PL	-	max (5nCK, 10ns) +PL	-	max (5nCK, 10ns) +PL	-	nCK	
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	max(5nCK, 1 0ns)	-	max(5nCK, 1 0ns)	-	max(5nCK, 1 0ns)	-	max (5nCK, 10ns)	-	nCK	
Power Down Timing											
Exit Power Down with DLL on to any valid command;Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max (4nCK, 6ns)	-	max (4nCK, 6ns)	-	max (4nCK, 6ns)	-	max (4nCK, 6ns)	-	nCK	
CKE minimum pulse width	tCKE	max (3nCK, 5ns)	-	max (3nCK, 5ns)	-	max (3nCK, 5ns)	-	max (3nCK, 5ns)	-	nCK	31,32
Command pass disable delay	tCPDED	4	-	4	-	4	-	4	-	nCK	
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	nCK	6
Timing of ACT command to Power Down entry	tACTPDEN	1	-	1	-	2	-	2	-	nCK	7
Timing of PRE or PREA command to Power Down entry	tPRPDEN	1	-	1	-	2	-	2	-	nCK	7
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL+4+1	-	RL+4+1	-	RL+4+1	-	RL+4+1	-	nCK	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL+4+(tWR/ tCK(avg))	-	WL+4+(tWR/ tCK(avg))	-	WL+4+(tWR/ tCK(avg))	-	WL+4+(tWR/ tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL+4+WR+ 1	-	WL+4+WR+ 1	-	WL+4+WR+ 1	-	WL+4+WR+ 1	-	nCK	5
Timing of WR command to Power Down entry (BC4MRS)	tWRP- BC4DEN	WL+2+(tWR/ tCK(avg))	-	WL+2+(tWR/ tCK(avg))	-	WL+2+(tWR/ tCK(avg))	-	WL+2+(tWR/ tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BC4MRS)	tWRAP- BC4DEN	WL+2+WR+ 1	-	WL+2+WR+ 1	-	WL+2+WR+ 1	-	WL+2+WR+ 1	-	nCK	5
Timing of REF command to Power Down entry	tREFPDEN	1	-	1	-	2	-	2	-	nCK	7
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-	nCK	
PDA Timing											
Mode Register Set command cycle time in PDA mode	tMRD_PDA	max(16nCK, 10ns)	-	max(16nCK, 10ns)	-	max(16nCK, 10ns)	-	max(16nCK, 10ns)	-	nCK	
Mode Register Set command update delay in PDA mode	tMOD_PDA	tMOD		tMOD		tMOD		tMOD		nCK	
ODT Timing											
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONAS	1.0	9.0	1.0	9.0	1.0	9.0	1.0	9.0	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFAS	1.0	9.0	1.0	9.0	1.0	9.0	1.0	9.0	ns	
RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	tCK(avg)	
Write Leveling Timing											
First DQS_t/DQS_n rising edge after write leveling mode is programmed	tWLMRD	40	-	40	-	40	-	40	-	nCK	12
DQS_t/DQS_n delay after write leveling mode is programmed	tWLDQSEN	25	-	25	-	25	-	25	-	nCK	12
Write leveling setup time from rising CK_t, CK_c crossing to rising DQS_t/DQS_n crossing	tWLS	0.13	-	0.13	-	0.13	-	0.13	-	tCK(avg)	
Write leveling hold time from rising DQS_t/ DQS_n crossing to rising CK_t, CK_crossing	tWLH	0.13	-	0.13	-	0.13	-	0.13	-	tCK(avg)	
Write leveling output delay	tWLO	0	9.5	0	9.5	0	9.5	0	9.5	ns	
Write leveling output error	tWLOE	0	2	0	2	0	2	0	2	ns	
CA Parity Timing											
Commands not guaranteed to be executed during this time	tPAR_UNKNOWN	-	PL	-	PL	-	PL	-	PL	nCK	
Delay from errant command to ALERT_n assertion	tPAR_ALERT_ON	-	PL+6ns	-	PL+6ns	-	PL+6ns	-	PL+6ns	nCK	
Pulse width of ALERT_n signal when asserted	tPAR_ALERT_PW	48	96	56	112	64	128	72	144	nCK	
Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode	tPAR_ALERT_RSP	-	43	-	50	-	57	-	64	nCK	
Parity Latency	PL	4		4		4		5		nCK	

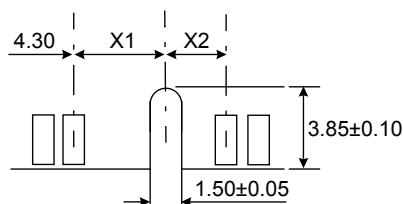
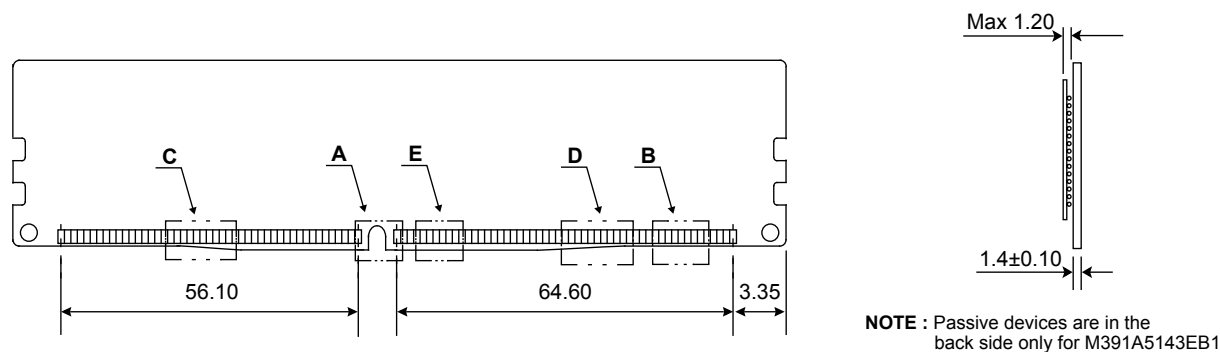
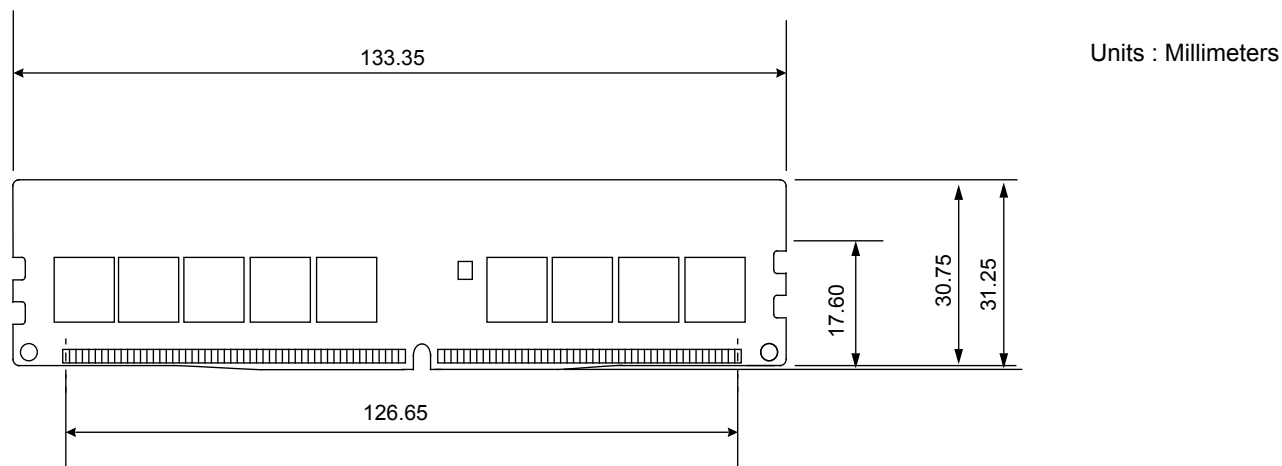
Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
CRC Error Reporting											
CRC error to ALERT_n latency	tCRC_ALERT	3	13	3	13	3	13	3	13	ns	
CRC ALERT_n pulse width	CRC_ALERT_PW	6	10	6	10	6	10	6	10	nCK	
Geardown timing											
Exit RESET from CKE HIGH to a valid MRS geardown (T2/Reset)	tXPR_GEAR	-	-	-	-	-	-	-	-		
CKE High Assert to Gear Down Enable time(T2/CKE)	tXS_GEAR	-	-	-	-	-	-	-	-		
MRS command to Sync pulse time(T3)	tSYNC_GEAR	-	-	-	-	-	-	-	-		27
Sync pulse to First valid command(T4)	tCMD_GEAR	-	-	-	-	-	-	-	-		27
Geardown setup time	tGEAR_setup	-	-	-	-	-	-	-	-	nCK	
Geardown hold time	tGEAR_hold	-	-	-	-	-	-	-	-	nCK	
tREFI											
tRFC1 (min)	2Gb	160	-	160	-	160	-	160	-	ns	34
	4Gb	260	-	260	-	260	-	260	-	ns	34
	8Gb	350	-	350	-	350	-	350	-	ns	34
	16Gb	550	-	550	-	550	-	550	-	ns	34
tRFC2 (min)	2Gb	110	-	110	-	110	-	110	-	ns	34
	4Gb	160	-	160	-	160	-	160	-	ns	34
	8Gb	260	-	260	-	260	-	260	-	ns	34
	16Gb	350	-	350	-	350	-	350	-	ns	34
tRFC4 (min)	2Gb	90	-	90	-	90	-	90	-	ns	34
	4Gb	110	-	110	-	110	-	110	-	ns	34
	8Gb	160	-	160	-	160	-	160	-	ns	34
	16Gb	260	-	260	-	260	-	260	-	ns	34

NOTE :

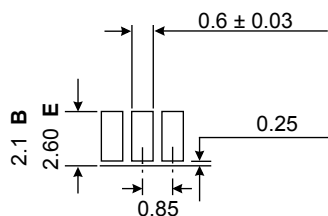
1. Start of internal write transaction is defined as follows :
For BL8 (Fixed by MRS and on-the-fly) : Rising clock edge 4 clock cycles after WL.
For BC4 (on-the-fly) : Rising clock edge 4 clock cycles after WL.
For BC4 (fixed by MRS) : Rising clock edge 2 clock cycles after WL.
2. A separate timing parameter will cover the delay from write to read when CRC and DM are simultaneously enabled
3. Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.
4. tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR/tCK to the next integer.
5. WR in clock cycles as programmed in MR0.
6. tREFI depends on TOPER.
7. CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.
8. For these parameters, the DDR4 SDRAM device supports $t_nPARAM[nCK] = RU\{tPARAM[ns]/tCK(avg)[ns]\}$, which is in clock cycles assuming all input clock jitter specifications are satisfied
9. When CRC and DM are both enabled, tWR_CRC_DM is used in place of tWR.
10. When CRC and DM are both enabled tWTR_S_CRC_DM is used in place of tWTR_S.
11. When CRC and DM are both enabled tWTR_L_CRC_DM is used in place of tWTR_L.
12. The max values are system dependent.
13. DQ to DQS total timing per group where the total includes the sum of deterministic and random timing terms for a specified BER. BER spec and measurement method are tbd.
14. The deterministic component of the total timing. Measurement method tbd.
15. DQ to DQ static offset relative to strobe per group. Measurement method tbd.
16. This parameter will be characterized and guaranteed by design.
17. When the device is operated with the input clock jitter, this parameter needs to be derated by the actual $tjit(per)_{total}$ of the input clock. (output deratings are relative to the SDRAM input clock). Example tbd.
18. DRAM DBI mode is off.
19. DRAM DBI mode is enabled. Applicable to x8 and x16 DRAM only.
20. tQSL describes the instantaneous differential output low pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge
21. tQSH describes the instantaneous differential output high pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge
22. There is no maximum cycle time limit besides the need to satisfy the refresh interval tREFI
23. tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge
24. tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge
25. Total jitter includes the sum of deterministic and random jitter terms for a specified BER. BER target and measurement method are tbd.
26. The deterministic jitter component out of the total jitter. This parameter is characterized and guaranteed by design.
27. This parameter has to be even number of clocks
28. When CRC and DM are both enabled, tWR_CRC_DM is used in place of tWR.
29. When CRC and DM are both enabled tWTR_S_CRC_DM is used in place of tWTR_S.
30. When CRC and DM are both enabled tWTR_L_CRC_DM is used in place of tWTR_L.
31. After CKE is registered LOW, CKE signal level shall be maintained below VILDC for tCKE specification (Low pulse width).
32. After CKE is registered HIGH, CKE signal level shall be maintained above VIHDC for tCKE specification (HIGH pulse width).
33. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.
34. Parameters apply from tCK(avg)min to tCK(avg)max at all standard JEDEC clock period values as stated in the Speed Bin Tables.
35. This parameter must keep consistency with Speed-Bin Tables .
36. DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate.
 $UI = tCK(avg).min/2$
37. applied when DRAM is in DLL ON mode.
38. Assume no jitter on input clock signals to the DRAM
39. Value is only valid for RZQ/7 RONNOM = 34 ohms
40. 1tCK toggle mode with setting MR4:A11 to 0
41. 2tCK toggle mode with setting MR4:A11 to 1, which is valid for DDR4-2400/2666/3200 speed grade.
42. 1tCK mode with setting MR4:A12 to 0
43. 2tCK mode with setting MR4:A12 to 1, which is valid for DDR4-2400/2666/3200 speed grade.
44. The maximum read preamble is bounded by tLZ(DQS)min on the left side and tDQSCK(max) on the right side.
45. DQ falling signal middle-point of transferring from High to Low to first rising edge of DQS diff-signal cross-point
46. last falling edge of DQS diff-signal cross-point to DQ rising signal middle-point of transferring from Low to High
47. VrefDQ value must be set to either its midpoint or Vcent_DQ(midpoint) in order to capture DQ0 or DQL0 low level for entering PDA mode.
48. The maximum read postamble is bound by tDQSCK(min) plus tQSH(min) on the left side and tHZ(DQS)max on the right side.
49. Reference level of DQ output signal is specified with a midpoint as a widest part of Output signal eye which should be approximately $0.7 * VDDQ$ as a center level of the static single-ended output peak-to-peak swing with a driver impedance of 34 ohms and an effective test load of 50 ohms to VTT = VDDQ .
50. For MR7 commands, the minimum delay to a subsequent non-MRS command is 5nCK.

17. Physical Dimensions

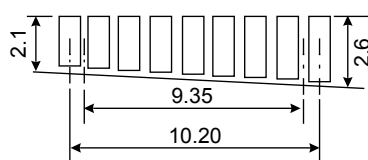
17.1 512Mbx8 based 512Mx72 Module (1 Rank) - M391A5143EB1



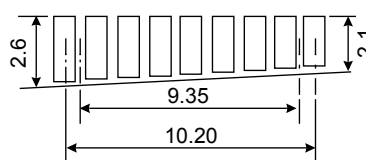
Detail A



Detail B, E



Detail C

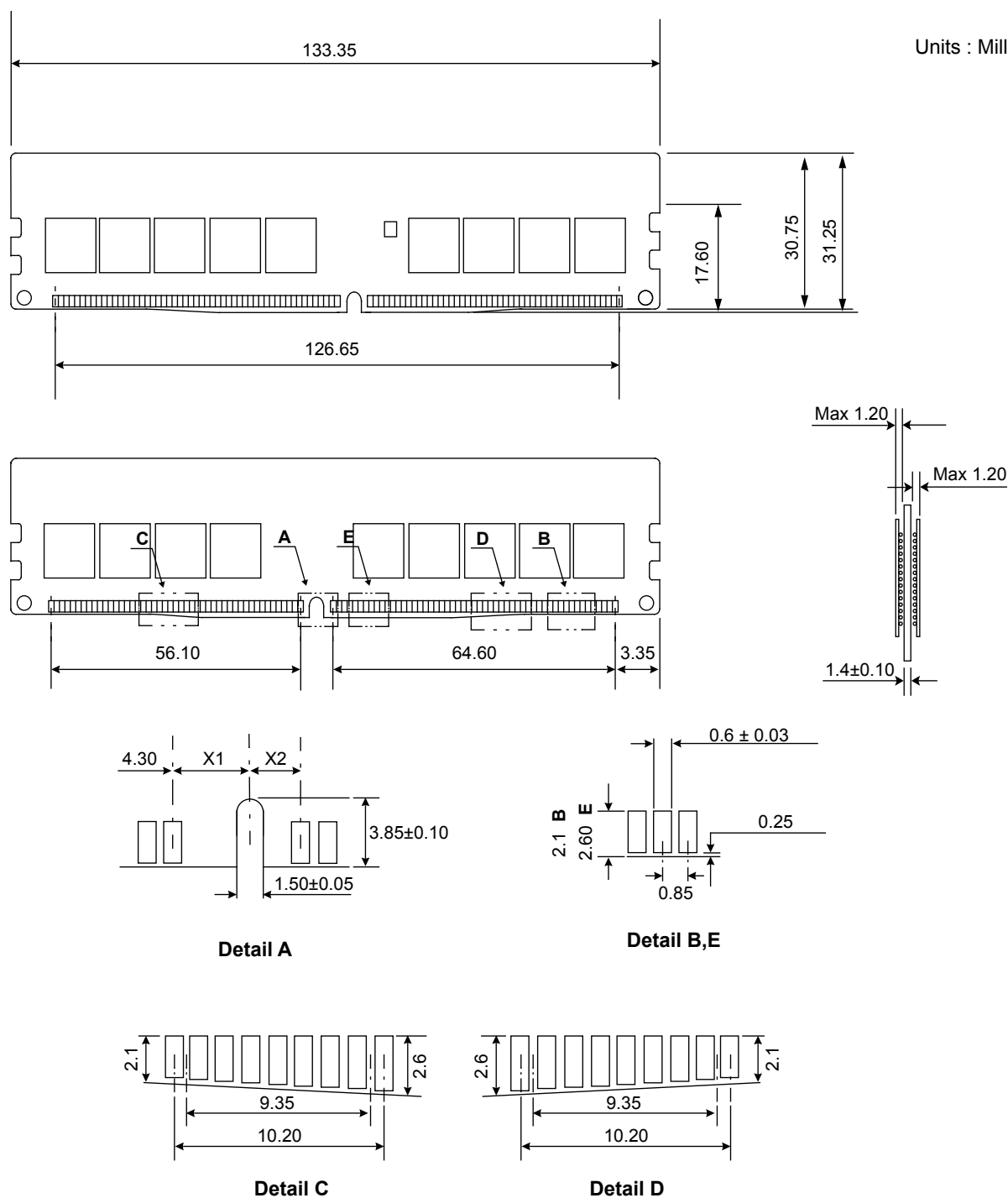


Detail D

The used device is 512M x8 DDR4 SDRAM, FBGA.
DDR4 SDRAM Part NO : K4A4G085WE-BC**

* **NOTE :** Tolerances on all dimensions ±0.15 unless otherwise specified.

17.2 512Mbx8 based 1Gx72 Module (2 Ranks) - M391A1G43EB1



The used device is 512M x8 DDR4 SDRAM, FBGA.
DDR4 SDRAM Part NO : K4A4G085WE-BC**

* **NOTE** : Tolerances on all dimensions ± 0.15 unless otherwise specified.