SERIAL PRESENCE DETECT

M386AAK40B40-CWD70

Composition : 2G x4 *36ea
Used component part # : K4ABG045WB-4CWDM00
# of rows in module : 2Rows
# of banks in component : 4Banks 4BG
Feature : 31.25mm height & double sided component
Refresh : 8K/64ms
Bin Sort : WD(DDR4 2666@CL=22)
RCD Vendor and Revision : IDT RCD B1(Gen2.0) , DB B0(Gen2.0)

Byte #	Function Described	Function Supported	Hex Value	Note
		CWD70	CWD70	
0	Number of Bytes Used / Number of Bytes in SPD Device / CRC Coverage	512B Total, 384B Used	23h	
1	SPD Revision	Ver 1.2	12h	
2	Key Byte / DRAM Device Type	DDR4 SDRAM	0Ch	
3	Key Byte / Module Type	LRDIMM	04h	
4	SDRAM Density and Banks	8Gb, 4BG&4Banks	85h	
5	SDRAM Addressing	Row bits 17,Column bits 10	29h	
6	SDRAM Package Type	3DS 4H	B2h	
7	SDRAM Optional Features	Unlimited MAC	08h	
8	SDRAM Thermal and Refresh Option	Reserved	00h	
9	Other SDRAM Optional Features	sPPR supported	60h	
10	Secondary SDRAM Package Type	Reserved	00h	
11	Module Nominal Voltage, VDD	1.2V	03h	
12	Module Organization	2Rx4	08h	
13	Module Memory Bus Width	64bit,ECC	0Bh	
14	Module Thermal Sensor	With TS	80h	
15	Extended Module Type	Reserved	00h	
16	Reserved	Reserved	00h	
17	Timebases	MTB 125ps, FTB 1ps	00h	
18	SDRAM Minimum Cycle Time(tckavg min)	0.750ns	06h	
19	SDRAM Minimum Cycle Time(tckavg max)	1.6ns	0Dh	
20	Cas Latency Supported, First Byte	11,12,13,14,15,16,17,18,19, 20,21,22,23	F0h	
21	Cas Latency Supported, Second Byte	11,12,13,14,15,16,17,18,19, 20,21,22,23	FFh	
22	Cas Latency Supported, Third Byte	11,12,13,14,15,16,17,18,19, 20,21,22,23	01h	
23	Cas Latency Supported, Fourth Byte	11,12,13,14,15,16,17,18,19, 20,21,22,23	00h	
24	Minimum Cas Latency Time (tAAmin)	16.5ns	84h	
25	Minimum RAS to CAS Delay Time(tRCD min)	14.25ns	72h	
26	Minimum Raw Precharge Delay Time(tRP min)	14.25ns	72h	
27	Upper Nibbles for tRASmin and tRCmin	tRAS=32ns, tRC=45.75ns	11h	
28	Minimum Active to Precharge Delay Time (tRASmin), Least Significant Byte	tRAS=32ns	00h	
29	Minimum Active to Active/Refresh Delay Time (tRCmin), Least Significant Byte	tRC=45.75ns	6Eh	
30	Minimum Refresh Recovery Delay Time (tRFC1min), LSB	350ns	F0h	
31	Minimum Refresh Recovery Delay Time (tRFC1min), MSB	350ns	0Ah	
32	Minimum Refresh Recovery Delay Time (tRFC2min), LSB	260ns	20h	
33	Minimum Refresh Recovery Delay Time (tRFC2min), MSB	260ns	08h	
34	Minimum Refresh Recovery Delay Time (tRFC4min), LSB	160ns	00h	
35	Minimum Refresh Recovery Delay Time (tRFC4min), MSB	160ns	05h	
36	Minimum Four Active Window Time (tFAWmin), Most Significant Nibble	12ns	00h	
37	Minimum Four Activate Window Time (tFAWmin), Least Significant Byte	12ns	60h	

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Byte #	Function Described	Function Supported	Hex Value	Note
		CWD70	CWD70	
38	Minimum Active to Active Delay Time (tRRD_smin), different Bank Group	3.0ns	18h	
39	Minimum Active to Active Delay Time (tRRD_Lmin), Same Bank Group	4.9ns	28h	
40	Minimum CAS to CAS Delay Time(tCCD_Lmin), same bank group	5ns	28h	
41	Upper Nibble for tWRmin	15ns	00h	
42	Minimum Write Recovery Time(tWRmin)	15ns	78h	
43	Upper Nibbles for tWTRmin	2.5ns	00h	
44	Minimum Write to Read Time(tWTR_smin), different bank group	2.5ns	14h	
45	Minimum Write to Read Time(tWTR_Lmin), same bank group	7.5ns	3Ch	
46~59	Reserved	Reserved	00h	
60	Connector to SDRAM Bit Mapping	DQ0-3	0Bh	
61	Connector to SDRAM Bit Mapping	DQ4-7	0Bh	
62	Connector to SDRAM Bit Mapping	DQ8-11	0Bh	
63	Connector to SDRAM Bit Mapping	DQ12-15	0Bh	
64	Connector to SDRAM Bit Mapping	DQ16-19	0Bh	
65	Connector to SDRAM Bit Mapping	DQ20-23	0Bh	
66	Connector to SDRAM Bit Mapping	DQ24-27	0Bh	
67	Connector to SDRAM Bit Mapping	DQ28-31	0Bh	
68	Connector to SDRAM Bit Mapping	CB0-3	0Bh	
69	Connector to SDRAM Bit Mapping	CB4-7	0Bh	
70	Connector to SDRAM Bit Mapping	DQ32-35	0Bh	
71	Connector to SDRAM Bit Mapping	DQ36-39	0Bh	
72	Connector to SDRAM Bit Mapping	DQ40~43	0Bh	
73	Connector to SDRAM Bit Mapping	DQ44-47	0Bh	
74	Connector to SDRAM Bit Mapping	DQ48-51	0Bh	
75	Connector to SDRAM Bit Mapping	DQ52-55	0Bh	
76	Connector to SDRAM Bit Mapping	DQ56-59	0Bh	
77	Connector to SDRAM Bit Mapping	DQ60-63	0Bh	
78~116	Reserved	reserved	00h	
117	Fine Offset for Minimum CAS to CAS Delay Time(tCCD_Lmin), same bank group	5ns	00h	
118	Fine Offset for Minimum Activate to Acticate Delay Time(tRRD_L_min), Same Bank Group	4.9ns	9Ch	
119	Fine Offset for Minimum Activate to Acticate Delay Time(tRRD_Smin), Different Bank Group	3.0ns	00h	
120	Fine Offset for Minimum Activate to Acticate/Refresh Delay Time(tRCmin)	45.75ns	00h	
121	Fine Offset for Minimum Row Precharge Delay Time(tRPmin)	14.25ns	00h	
122	Fine Offset for Minimum RAS to CAS Delay Time(tRCD_min)	14.25ns	00h	
123	Fine Offset for Minimum CAS Latency Delay Time(tAA_min)	16.5ns	00h	
124	Fine Offset for DRAM Maximum Cycle Time(tCKAVG_max)	1.6ns	E7h	
125	Fine Offset for DRAM Minimum Cycle Time(tCKAVG_min)	0.750ns	00h	
126	Cyclical Redundancy Code	-	C7h	
127	Cyclical Redundancy Code	-	5Ah	
128	Raw Card Extension, Module Nominal Height	R/C A 0.0, 31.25mm	11h	
129	Module Maximum Thickness	(Each side)1<thickness&l t;2mm	11h	
130	Reference Raw Card Used	R/C A 0.0	00h	
131	DIMM Module Attributes	RCD2 2row 1register	19h	
132	LRDIMM Thermal Heat Spreader Solution	W/O H/S	00h	
133	Register and Data Buffer Manufacturer ID Code, Least Signficant Byte	IDT	80h	
134	Register and Data Buffer Manufacturer ID Code, Most Signficant Byte	IDT	B3h	

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		CWD70	CWD70	
135	Register Revision Number	IDT B1	51h	
136	Address Mapping from Register to DRAM	Mirrored	01h	
137	Register Ouput Drive Strength for Control	CMD/ADD Strong, CS/CKE/ODT : Moderate	65h	
138	Register Output Strength for CK	Moderate	05h	
139	Data Buffer Revision Number	IDT RCD(B0), DB(B0)	B0h	
140	DRAM VrefDQ for Package Rank 0	R1 69.75% , R2 54.75%	0Fh	
141	DRAM VrefDQ for Package Rank 1	R1 69.75% , R2 54.75%	0Fh	
142	DRAM VrefDQ for Package Rank 2	R1: 60% , R2: 45%	00h	
143	DRAM VrefDQ for Package Rank 3	R1: 60% , R2: 45%	00h	
144	Data Burrer VrefDQ for DRAM Interface	VrefDQ value	12h	
145	Data Buffer MDQ Drive Strength and RTT for data rate < 1866	34ohm, 48ohm	15h	
146	Data Buffer MDQ Drive Strength and RTT for data rate < 2400	34ohm, 48ohm	15h	
147	Data Buffer MDQ Drive Strength and RTT for data rate < 3200	34ohm, 48ohm	15h	
148	DRAM Drive Strength (for data rates 1866 < data rate < 2400, and 2400 < data rate < 3200)	34ohm, 34ohm, 34ohm	00h	
149	DRAM ODT (RTT_WR and RTT_NOM) for data rate < 1866	240ohm,240ohm	14h	
150	DRAM ODT (RTT_WR and RTT_NOM) for 1866 < data rate <2400	240ohm,240ohm	14h	
151	DRAM ODT (RTT_WR and RTT_NOM) for 2400 < data rate < 3200	240ohm,240ohm	14h	
152	DRAM ODT (RTT_PARK) for data rate < 1866	Disabled, 60ohm	01h	
153	DRAM ODT (RTT_PARK) for data rate 1866 < data rate < 2400	Disabled, 60ohm	01h	
154	DRAM ODT (RTT_PARK) for data rate 2400 < data rate < 3200	Disabled, 60ohm	01h	
155~253	Reserved	Reserved	00h	
254	Cyclical Redundancy Code	-	2Bh	
255	Cyclical Redundancy Code	-	3Fh	
256~319	Reserved	Reserved	00h	
320	Module Manufacturer's ID Code, Least Significant Byte	Samsung	80h	
321	Module Manufacturer's ID Code, Most Significant Byte	Samsung	CEh	
322	Module Manufactoring Location	Samsung	00h	
323	Module Manufactoring Date	Year	00h	
324	Module Manufactoring Date	Week	00h	
325	Module Serial Number	-	00h	
326	Module Serial Number	-	00h	
327	Module Serial Number	-	00h	
328	Module Serial Number	-	00h	
329	Module Part Number	M	4Dh	
330	Module Part Number	3	33h	
331	Module Part Number	8	38h	
332	Module Part Number	6	36h	
333	Module Part Number	A	41h	
334	Module Part Number	A	41h	
335	Module Part Number	K	4Bh	
336	Module Part Number	4	34h	
337	Module Part Number	0	30h	
338	Module Part Number	B-die	42h	
339	Module Part Number	4	34h	
340	Module Part Number	0	30h	

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		CWD70	CWD70	
341	Module Part Number	-	2Dh	
342	Module Part Number	C	43h	
343	Module Part Number	W	57h	
344	Module Part Number	D	44h	
345	Module Part Number	Blank	20h	
346	Module Part Number	Blank	20h	
347	Module Part Number	Blank	20h	
348	Module Part Number	Blank	20h	
349	Module Revision Code	0.0	00h	
350	DRAM Manufacturer's ID Code, Least Sgnificant Byte	SAMSUNG	80h	
351	DRAM Manufacturer's ID Code, Most Sgnificant Byte	SAMSUNG	CEh	
352	DRAM Stepping	Ver 0.0	00h	
353~380	Module Manufacturer's Specific Data	Reserved	00h	
381	Module Manufacturer's Specific Data	Reserved	DDh	
382~383	Reserved	Reserved	00h	
384~511	End User Programmable	Reserved	00h	

Note : 4. Y : Clock for Memory Buffer