

SERIAL PRESENCE DETECT

M392A2K43BB0-CPB00

Organization : 1G x 72
 Composition : 1Gx8 *18ea
 Used component part # : K4A8G085WB-BCPB00
 # of rows in module : 1Row
 # of banks in component : 4Banks 4BG
 Feature : 18.75mm height & double sided component
 Refresh : 8K/64ms
 Bin Sort : PB(DDR4 2133@CL=15)
 RCD Vendor and Revision : IDT C0 0.92ver

| Byte # | Function Described | Function Supported | Hex Value | Note |
|--------|--|-----------------------------|-----------|------|
| | | CPB00 | CPB00 | |
| 0 | Number of Bytes Used / Number of Bytes in SPD Device / CRC Coverage | 512B Total, 384B Used | 23h | |
| 1 | SPD Revision | Ver 1.0 | 10h | |
| 2 | Key Byte / DRAM Device Type | DDR4 SDRAM | 0Ch | |
| 3 | Key Byte / Module Type | RDIMM | 01h | |
| 4 | SDRAM Density and Banks | 8Gb, 4BG&4Banks | 85h | |
| 5 | SDRAM Addressing | Row bits 16, Column bits 10 | 21h | |
| 6 | SDRAM Device Type | Monolithic Device | 00h | |
| 7 | SDRAM Optional Features | Unlimited MAC | 08h | |
| 8 | SDRAM Thermal and Refresh Option | Reserved | 00h | |
| 9 | Other SDRAM Optional Features | PPR supported | 40h | |
| 10 | Reserved | Reserved | 00h | |
| 11 | Module Nominal Voltage, VDD | 1.2V | 03h | |
| 12 | Module Organization | 2Rx8 | 09h | |
| 13 | Module Memory Bus Width | 64bit,ECC | 0Bh | |
| 14 | Module Thermal Sensor | With TS | 80h | |
| 15-16 | Reserved | Reserved | 00h | |
| 17 | Timebases | MTB 125ps, FTB 1ps | 00h | |
| 18 | SDRAM Minimum Cycle Time(tckavg min) | 0.938ns | 08h | |
| 19 | SDRAM Minimum Cycle Time(tckavg max) | 1.5ns | 0Ch | |
| 20 | Cas Latency Supported, First Byte | 10,11,12,13,14,15,16 | F8h | |
| 21 | Cas Latency Supported, Second Byte | 10,11,12,13,14,15,16 | 03h | |
| 22 | Cas Latency Supported, Third Byte | 10,11,12,13,14,15,16 | 00h | |
| 23 | Cas Latency Supported, Fourth Byte | 10,11,12,13,14,15,16 | 00h | |
| 24 | Minimum Cas Latency Time (tAAmin) | 13.75ns | 6Eh | |
| 25 | Minimum RAS to CAS Delay Time(tRCD min) | 13.75ns | 6Eh | |
| 26 | Minimum Raw Precharge Delay Time(tRP min) | 13.75ns | 6Eh | |
| 27 | Upper Nibbles for tRASmin and tRCmin | tRAS=33ns, tRC=46.75ns | 11h | |
| 28 | Minimum Active to Precharge Delay Time (tRASmin), Least Significant Byte | tRAS=33ns | 08h | |
| 29 | Minimum Active to Active/Refresh Delay Time (tRCmin), Least Significant Byte | tRC=46.75ns | 76h | |
| 30 | Minimum Refresh Recovery Delay Time (tRFC1min), LSB | 350ns | F0h | |
| 31 | Minimum Refresh Recovery Delay Time (tRFC1min), MSB | 350ns | 0Ah | |
| 32 | Minimum Refresh Recovery Delay Time (tRFC2min), LSB | 260ns | 20h | |
| 33 | Minimum Refresh Recovery Delay Time (tRFC2min), MSB | 260ns | 08h | |
| 34 | Minimum Refresh Recovery Delay Time (tRFC4min), LSB | 160ns | 00h | |
| 35 | Minimum Refresh Recovery Delay Time (tRFC4min), MSB | 160ns | 05h | |
| 36 | Minimum Four Active Window Time (tFAWmin), Most Significant Nibble | 21ns | 00h | |
| 37 | Minimum Four Activate Window Time (tFAWmin), Least Significant Byte | 21ns | A8h | |
| 38 | Minimum Active to Active Delay Time (tRRD_smin), different Bank Group | 3.7ns | 1Eh | |
| 39 | Minimum Active to Active Delay Time (tRRD_Lmin), Same Bank Group | 5.3ns | 2Bh | |
| 40 | Minimum CAS to CAS Delay Time(tCCD_Lmin), same bank group | 5.625ns | 2Eh | |

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|---------|--|---|-----------|------|
| | | CPB00 | CPB00 | |
| 41-59 | Reserved | reserved | 00h | |
| 60 | Connector to SDRAM Bit Mapping | DQ0-3 (VLP R H0) | 16h | |
| 61 | Connector to SDRAM Bit Mapping | DQ4-7 (VLP R H0) | 36h | |
| 62 | Connector to SDRAM Bit Mapping | DQ8-11 (VLP R H0) | 16h | |
| 63 | Connector to SDRAM Bit Mapping | DQ12-15 (VLP R H0) | 36h | |
| 64 | Connector to SDRAM Bit Mapping | DQ16-19 (VLP R H0) | 0Ch | |
| 65 | Connector to SDRAM Bit Mapping | DQ20-23 (VLP R H0) | 2Ch | |
| 66 | Connector to SDRAM Bit Mapping | DQ24-27 (VLP R H0) | 0Ch | |
| 67 | Connector to SDRAM Bit Mapping | DQ28-31 (VLP R H0) | 2Ch | |
| 68 | Connector to SDRAM Bit Mapping | CB0-3 (VLP R H0) | 0Ch | |
| 69 | Connector to SDRAM Bit Mapping | CB4-7 (VLP R H0) | 2Ch | |
| 70 | Connector to SDRAM Bit Mapping | DQ32-35 (VLP R H0) | 16h | |
| 71 | Connector to SDRAM Bit Mapping | DQ36-39 (VLP R H0) | 36h | |
| 72 | Connector to SDRAM Bit Mapping | DQ40-43 (VLP R H0) | 0Ch | |
| 73 | Connector to SDRAM Bit Mapping | DQ44-47 (VLP R H0) | 2Bh | |
| 74 | Connector to SDRAM Bit Mapping | DQ48-51 (VLP R H0) | 0Ch | |
| 75 | Connector to SDRAM Bit Mapping | DQ52-55 (VLP R H0) | 2Ch | |
| 76 | Connector to SDRAM Bit Mapping | DQ56-59 (VLP R H0) | 0Ch | |
| 77 | Connector to SDRAM Bit Mapping | DQ60-63 (VLP R H0) | 2Ch | |
| 78-116 | Reserved | reserved | 00h | |
| 117 | Fine Offset for Minimum CAS to CAS Delay Time(tCCD_Lmin), same bank group | 5.625ns | 83h | |
| 118 | Fine Offset for Minimum Activate to Acticate Delay Time(tRRD_L_min), Same Bank Group | 5.3ns | B5h | |
| 119 | Fine Offset for Minimum Activate to Acticate Delay Time(tRRD_Smin), Different Bank Group | 3.7ns | CEh | |
| 120 | Fine Offset for Minimum Activate to Acticate/Refresh Delay Time(tRCmin) | 46.75ns | 00h | |
| 121 | Fine Offset for Minimum Row Precharge Delay Time(tRPmin) | 13.75ns | 00h | |
| 122 | Fine Offset for Minimum RAS to CAS Delay Time(tRCD_min) | 13.75ns | 00h | |
| 123 | Fine Offset for Minimum CAS Latency Delay Time(tAA_min) | 13.75ns | 00h | |
| 124 | Fine Offset for DRAM Maximum Cycle Time(tCKAVG_max) | 1.5ns | 00h | |
| 125 | Fine Offset for DRAM Minimum Cycle Time(tCKAVG_min) | 0.938ns | C2h | |
| 126 | Cyclical Redundancy Code | - | 75h | |
| 127 | Cyclical Redundancy Code | - | 94h | |
| 128 | Raw Card Extension, Module Nominal Height | R/C H 0.0, 18.75mm | 04h | |
| 129 | Module Maximum Thickness | (Each side)1<t;thickness&l t;2mm | 11h | |
| 130 | Reference Raw Card Used | R/C H 0.0 | 07h | |
| 131 | DIMM Module Attributes | 1row 1register | 05h | |
| 132 | RDIMM Thermal Heat Spreader Solution | W/O H/S | 00h | |
| 133 | Register Manufacturer ID Code, Least Significant Byte | IDT | 80h | |
| 134 | Register Manufacturer ID Code, Most Significant Byte | IDT | B3h | |
| 135 | Register Revision Number | IDT C0 | 30h | |
| 136 | Address Mapping from Register to DRAM | Mirrored | 01h | |
| 137 | Register Ouput Drive Strength for Control | CMD/ADD : Moderate, CS/CKE/ ODT : Light | 10h | |
| 138 | Register Output Strength for CK | Light | 00h | |
| 139-253 | Reserved | Reserved | 00h | |
| 254 | Cyclical Redundancy Code | - | AAh | |
| 255 | Cyclical Redundancy Code | - | C3h | |

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|---------|---|--------------------|-----------|------|
| | | CPB00 | CPB00 | |
| 256-319 | Reserved | Reserved | 00h | |
| 320 | Module Manufacturer's ID Code, Least Significant Byte | Samsung | 80h | |
| 321 | Module Manufacturer's ID Code, Most Significant Byte | Samsung | CEh | |
| 322 | Module Manufacturing Location | Samsung | 00h | |
| 323 | Module Manufacturing Date | Year | 00h | |
| 324 | Module Manufacturing Date | Week | 00h | |
| 325 | Module Serial Number | - | 00h | |
| 326 | Module Serial Number | - | 00h | |
| 327 | Module Serial Number | - | 00h | |
| 328 | Module Serial Number | - | 00h | |
| 329 | Module Part Number | M | 4Dh | |
| 330 | Module Part Number | 3 | 33h | |
| 331 | Module Part Number | 9 | 39h | |
| 332 | Module Part Number | 2 | 32h | |
| 333 | Module Part Number | A | 41h | |
| 334 | Module Part Number | 2 | 32h | |
| 335 | Module Part Number | K | 4Bh | |
| 336 | Module Part Number | 4 | 34h | |
| 337 | Module Part Number | 3 | 33h | |
| 338 | Module Part Number | B-die | 42h | |
| 339 | Module Part Number | B | 42h | |
| 340 | Module Part Number | 0 | 30h | |
| 341 | Module Part Number | - | 2Dh | |
| 342 | Module Part Number | C | 43h | |
| 343 | Module Part Number | P | 50h | |
| 344 | Module Part Number | B | 42h | |
| 345 | Module Part Number | Blank | 20h | |
| 346 | Module Part Number | Blank | 20h | |
| 347 | Module Part Number | Blank | 20h | |
| 348 | Module Part Number | Blank | 20h | |
| 349 | Module Revision Code | 0.0 | 00h | |
| 350 | DRAM Manufacturer's ID Code, Least Sgnificant Byte | SAMSUNG | 80h | |
| 351 | DRAM Manufacturer's ID Code, Most Sgnificant Byte | SAMSUNG | CEh | |
| 352 | DRAM Stepping | Ver 0.0 | 00h | |
| 353-381 | Module Manufacturer's Specific Data | Reserved | 00h | |
| 382-383 | Reserved | Reserved | 00h | |
| 384-511 | End User Programmable | Reserved | 00h | |

Note : 1. ### #####.
 2. ### #####.
 3. ### #####.