SERIAL PRESENCE DETECT

M393A2K43CB2-CTD60

Organization : 1G x 72
Composition : 1Gb x8 *18ea
Used component part # : K4A8G085WC-BCTDM00
# of rows in module : 2Row
# of banks in component : 4Banks 4BG
Feature : 31.25mm height & double sided component
Refresh : 8K/64ms
Bin Sort : TD(DDR4 2666@CL=19)
RCD Vendor and Revision : Montage A0(Gen. 2.0), PCB Rev.2.0

Byte #	Function Described	Function Supported	Hex Value	Note
		CTD60	CTD60	
0	Number of Bytes Used / Number of Bytes in SPD Device / CRC Coverage	512B Total, 384B Used	23h	
1	SPD Revision	Ver 1.2	12h	
2	Key Byte / DRAM Device Type	DDR4 SDRAM	0Ch	
3	Key Byte / Module Type	RDIMM	01h	
4	SDRAM Density and Banks	8Gb, 4BG&4Banks	85h	
5	SDRAM Addressing	Row bits 16, Column bits 10	21h	
6	SDRAM Device Type	Monolithinc Device	00h	
7	SDRAM Optional Features	Unlimited MAC	08h	
8	SDRAM Thermal and Refresh Option	Reserved	00h	
9	Other SDRAM Optional Features	sPPR supported	60h	
10	Secondary SDRAM Package Type	Reserved	00h	
11	Module Nominal Voltage, VDD	1.2V	03h	
12	Module Organization	2Rx8	09h	
13	Module Memory Bus Width	64bit,ECC	0Bh	
14	Module Thermal Sensor	With TS	80h	
15	Extended Module Type	Reserved	00h	
16	Reserved	Reserved	00h	
17	Timebases	MTB 125ps, FTB 1ps	00h	
18	SDRAM Minimum Cycle Time(tckavg min)	0.750ns	06h	
19	SDRAM Minimum Cycle Time(tckavg max)	1.6ns	0Dh	
20	Cas Latency Supported, First Byte	10,11,12,13,14,15,16,17,18, 19,20	F8h	
21	Cas Latency Supported, Second Byte	10,11,12,13,14,15,16,17,18, 19,20	3Fh	
22	Cas Latency Supported, Third Byte	10,11,12,13,14,15,16,17,18, 19,20	00h	
23	Cas Latency Supported, Fourth Byte	10,11,12,13,14,15,16,17,18, 19,20	00h	
24	Minimum Cas Latency Time (tAAmin)	13.75ns	6Eh	
25	Minimum RAS to CAS Delay Time(tRCD min)	13.75ns	6Eh	
26	Minimum Raw Precharge Delay Time(tRP min)	13.75ns	6Eh	
27	Upper Nibbles for tRASmin and tRCmin	tRAS=32ns, tRC=45.75ns	11h	
28	Minimum Active to Precharge Delay Time (tRASmin), Least Significant Byte	tRAS=32ns	00h	
29	Minimum Active to Active/Refresh Delay Time (tRCmin), Least Significant Byte	tRC=45.75ns	6Eh	
30	Minimum Refresh Recovery Delay Time (tRFC1min), LSB	350ns	F0h	
31	Minimum Refresh Recovery Delay Time (tRFC1min), MSB	350ns	0Ah	
32	Minimum Refresh Recovery Delay Time (tRFC2min), LSB	260ns	20h	
33	Minimum Refresh Recovery Delay Time (tRFC2min), MSB	260ns	08h	
34	Minimum Refresh Recovery Delay Time (tRFC4min), LSB	160ns	00h	
35	Minimum Refresh Recovery Delay Time (tRFC4min), MSB	160ns	05h	
36	Minimum Four Active Window Time (tFAWmin), Most Significant Nibble	21ns	00h	
37	Minimum Four Activate Window Time (tFAWmin), Least Significant Byte	21ns	A8h	
38	Minimum Active to Active Delay Time (tRRD_smin), different Bank Group	3.0ns	18h	
39	Minimum Active to Active Delay Time (tRRD_Lmin), Same Bank Group	4.9ns	28h	

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		CTD60	CTD60	
40	Minimum CAS to CAS Delay Time(tCCD_Lmin), same bank group	5ns	28h	
41	Upper Nibble for tWRmin	15ns	00h	
42	Minimum Write Recovery Time(tWRmin)	15ns	78h	
43	Upper Nibbles for tWTRmin	2.5ns	00h	
44	Minimum Write to Read Time(tWTR_smin), different bank group	2.5ns	14h	
45	Minimum Write to Read Time(tWTR_Lmin), same bank group	7.5ns	3Ch	
46~59	Reserved	Reserved	00h	
60	Connector to SDRAM Bit Mapping	DQ0, DQ1, DQ2, DQ3(R/C E)	0Ch	
61	Connector to SDRAM Bit Mapping	DQ4, DQ5, DQ6, DQ7(R/C E)	2Ch	
62	Connector to SDRAM Bit Mapping	DQ8, DQ9, DQ10, DQ11(R/C E)	0Ch	
63	Connector to SDRAM Bit Mapping	DQ12, DQ13, DQ14, DQ15(R/C E)	2Ch	
64	Connector to SDRAM Bit Mapping	DQ16, DQ17, DQ18, DQ19(R/C E)	0Ch	
65	Connector to SDRAM Bit Mapping	DQ20, DQ21, DQ22, DQ23(R/C E)	2Ch	
66	Connector to SDRAM Bit Mapping	DQ24, DQ25, DQ26, DQ27(R/C E)	0Ch	
67	Connector to SDRAM Bit Mapping	DQ28, DQ29, DQ30, DQ31(R/C E)	2Ch	
68	Connector to SDRAM Bit Mapping	CB0, CB1, CB2, CB3(R/C E)	0Ch	
69	Connector to SDRAM Bit Mapping	CB4, CB5, CB6, CB7(R/C E)	2Ch	
70	Connector to SDRAM Bit Mapping	DQ32, DQ33, DQ34, DQ35(R/C E)	0Ch	
71	Connector to SDRAM Bit Mapping	DQ36, DQ37, DQ38, DQ39(R/C E)	2Ch	
72	Connector to SDRAM Bit Mapping	DQ40, DQ41, DQ42, DQ43(R/C E)	0Ch	
73	Connector to SDRAM Bit Mapping	DQ44, DQ45, DQ46, DQ47(R/C E)	2Ch	
74	Connector to SDRAM Bit Mapping	DQ48, DQ49, DQ50, DQ51(R/C E)	0Ch	
75	Connector to SDRAM Bit Mapping	DQ52, DQ53, DQ54, DQ55(R/C E)	2Ch	
76	Connector to SDRAM Bit Mapping	DQ56, DQ57, DQ58, DQ59(R/C E)	0Ch	
77	Connector to SDRAM Bit Mapping	DQ60, DQ61, DQ62, DQ63(R/C E)	2Ch	
78~116	Reserved	reserved	00h	
117	Fine Offset for Minimum CAS to CAS Delay Time(tCCD_Lmin), same bank group	5ns	00h	
118	Fine Offset for Minimum Activate to Acticate Delay Time(tRRD_L_min), Same Bank Group	4.9ns	9Ch	
119	Fine Offset for Minimum Activate to Acticate Delay Time(tRRD_Smin), Different Bank Group	3.0ns	00h	
120	Fine Offset for Minimum Activate to Acticate/Refresh Delay Time(tRCmin)	45.75ns	00h	
121	Fine Offset for Minimum Row Precharge Delay Time(tRPmin)	13.75ns	00h	
122	Fine Offset for Minimum RAS to CAS Delay Time(tRCD_min)	13.75ns	00h	
123	Fine Offset for Minimum CAS Latency Delay Time(tAA_min)	13.75ns	00h	
124	Fine Offset for DRAM Maximum Cycle Time(tCKAVG_max)	1.6ns	E7h	
125	Fine Offset for DRAM Minimum Cycle Time(tCKAVG_min)	0.750ns	00h	
126	Cyclical Redundancy Code	-	DBh	
127	Cyclical Redundancy Code	-	39h	
128	Raw Card Extension, Module Nominal Height	R/C E 2.0 , 31.25mm	11h	
129	Module Maximum Thickness	(Each side)1<thickness&l t;2mm	11h	
130	Reference Raw Card Used	R/C E 2.0	44h	
131	DIMM Module Attributes	RCD2 1row 1register	15h	
132	RDIMM Thermal Heat Spreader Solution	W/O H/S	00h	
133	Register Manufacturer ID Code, Least Signficant Byte	MONTAGE	86h	
134	Register Manufacturer ID Code, Most Signficant Byte	MONTAGE	32h	
135	Register Revision Number	Montage A0	A0h	
136	Address Mapping from Register to DRAM	Mirrored	01h	

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		CTD60	CTD60	
137	Register Ouput Drive Strength for Control	CMD/ADD : Moderate, CS/CKE/ ODT : Light	10h	
138	Register Output Strength for CK	Light	00h	
139~253	Reserved	Reserved	00h	
254	Cyclical Redundancy Code	-	D8h	
255	Cyclical Redundancy Code	-	79h	
256~319	Reserved	Reserved	00h	
320	Module Manufacturer's ID Code, Least Significant Byte	Samsung	80h	
321	Module Manufacturer's ID Code, Most Significant Byte	Samsung	CEh	
322	Module Manufactoring Location	Samsung	00h	
323	Module Manufactoring Date	Year	00h	
324	Module Manufactoring Date	Week	00h	
325	Module Serial Number	-	00h	
326	Module Serial Number	-	00h	
327	Module Serial Number	-	00h	
328	Module Serial Number	-	00h	
329	Module Part Number	M	4Dh	
330	Module Part Number	3	33h	
331	Module Part Number	9	39h	
332	Module Part Number	3	33h	
333	Module Part Number	A	41h	
334	Module Part Number	2	32h	
335	Module Part Number	K	4Bh	
336	Module Part Number	4	34h	
337	Module Part Number	3	33h	
338	Module Part Number	C-die	43h	
339	Module Part Number	B	42h	
340	Module Part Number	2	32h	
341	Module Part Number	-	2Dh	
342	Module Part Number	C	43h	
343	Module Part Number	T	54h	
344	Module Part Number	D	44h	
345	Module Part Number	Blank	20h	
346	Module Part Number	Blank	20h	
347	Module Part Number	Blank	20h	
348	Module Part Number	Blank	20h	
349	Module Revision Code	0.0	00h	
350	DRAM Manufacturer's ID Code, Least Sgnificant Byte	SAMSUNG	80h	
351	DRAM Manufacturer's ID Code, Most Sgnificant Byte	SAMSUNG	CEh	
352	DRAM Stepping	Ver 0.0	00h	
353~380	Module Manufacturer's Specific Data	Reserved	00h	
381	Module Manufacturer's Specific Data	Reserved	DDh	
382~383	Reserved	Reserved	00h	
384~511	End User Programmable	Reserved	00h	

Note : 1. ??? ?????.
2. ??? ?????.

3. ??? ?????.