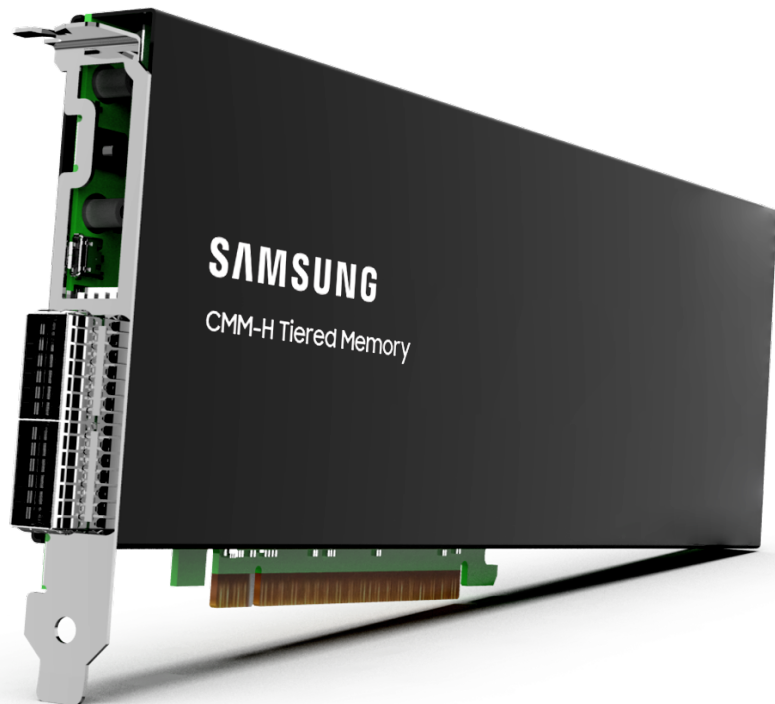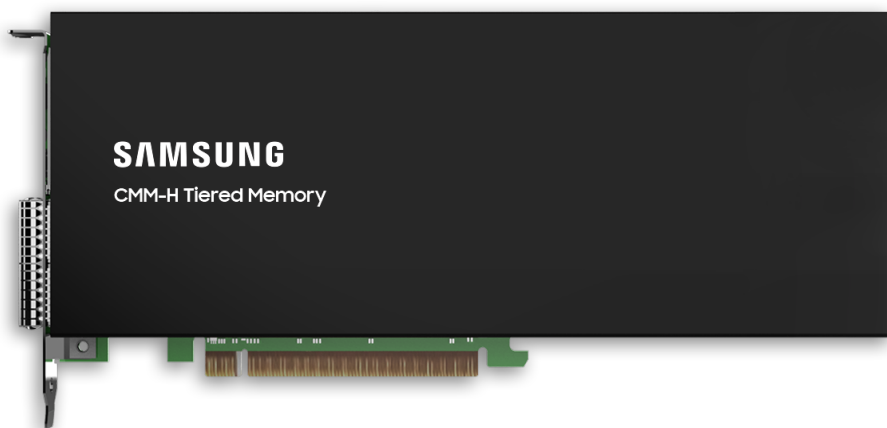# SAMSUNG

CMM-H Tiered Memory
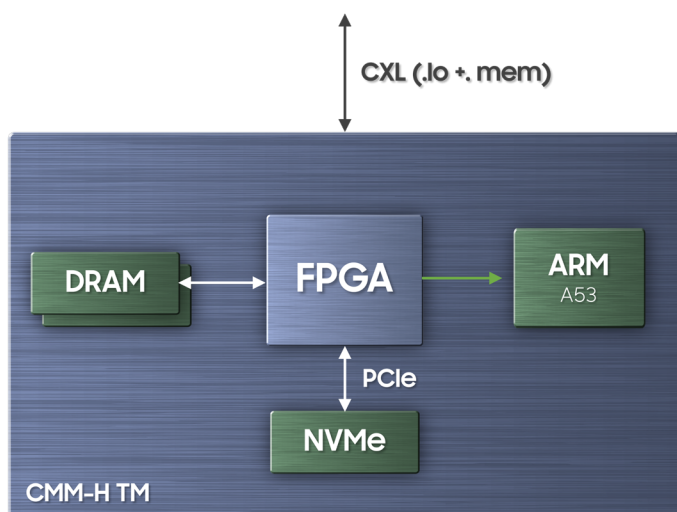
Data Sheet

Memory Solutions lab

Overview

The CMM-H features Samsung's high-performance DRAM, coupled with NAND Flash, and a CXL Type 3 interface. These technological characteristics are combined to offer a cost-effective memory expansion device. It presents large NUMA nodes with existing Linux kernel framework and seamlessly integrates with applications without the need for modification.
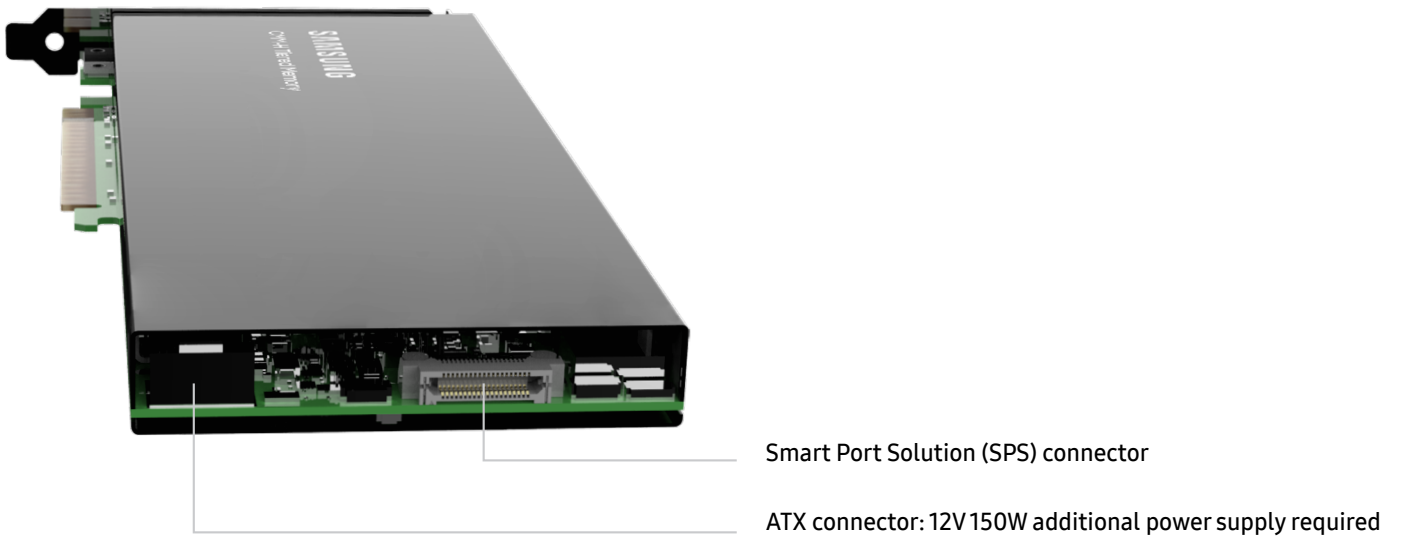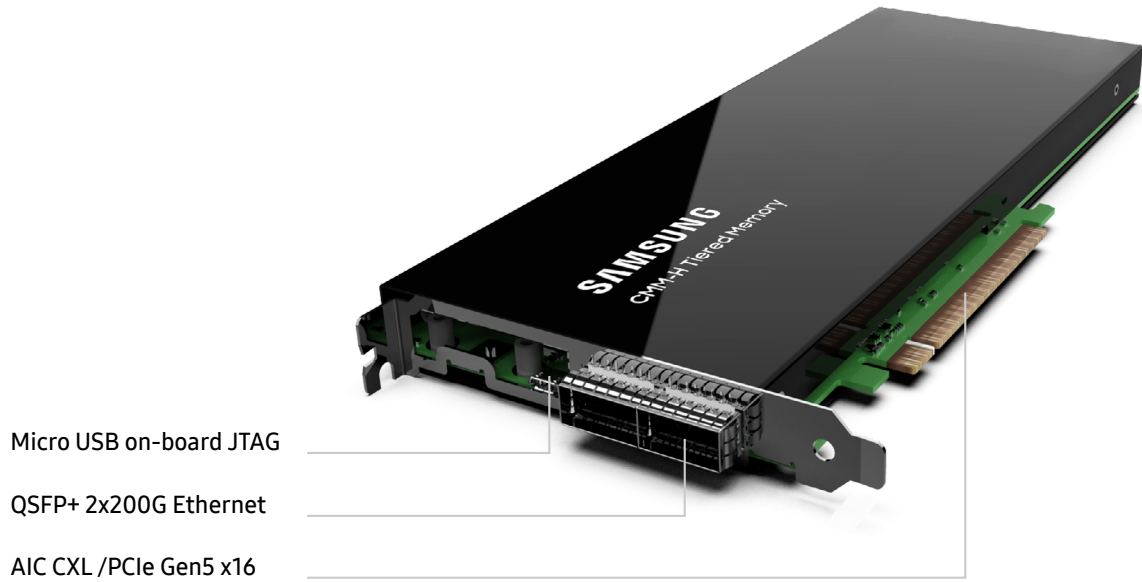

The CMM-H utilizes the combination of small amount of DRAM and large capacity NAND Flash to provide a large volatile memory capacity. The Tiered Memory IP manages the DRAM as a device cache, it prefetches and keeps hot pages in the DRAM thereby avoiding long NAND read latencies. The device cache is transparent to the Host.

The Host may send cache hints to the device via the Host CMM-H API which sends messages to the device via CXL.io.

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Device Hardware: Connectors

Micro USB on-board JTAG

QSFP+ 2x200G Ethernet

AIC CXL /PCIe Gen5 x16

Smart Port Solution (SPS) connector

ATX connector: 12V 150W additional power supply required

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Technical specifications

Features	Specifications
Advertised Capacity	1 TB volatile memory
Host Interface	PCIe Gen5 x16
	CXL 1.1, 2.0
	Type 3 device - CXL.io + CXL.mem
Device Memory	1 TB PCIe Gen4 x4 NVMe SSD
	48 GB DDR4
Device FPGA	Intel Altera Agilex 7
	Quad-core Arm Cortex-A53
Form Factor	Add-in Card (AIC)
	Single slot, Full Height, ¾ length

For more information

For more information about the Samsung Semiconductor products, visit **semiconductor.samsung.com.**

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