

DDR3 SDRAM Specification

Device Operation & Timing Diagram

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1. Functional Description

1.1 Simplified State Diagram

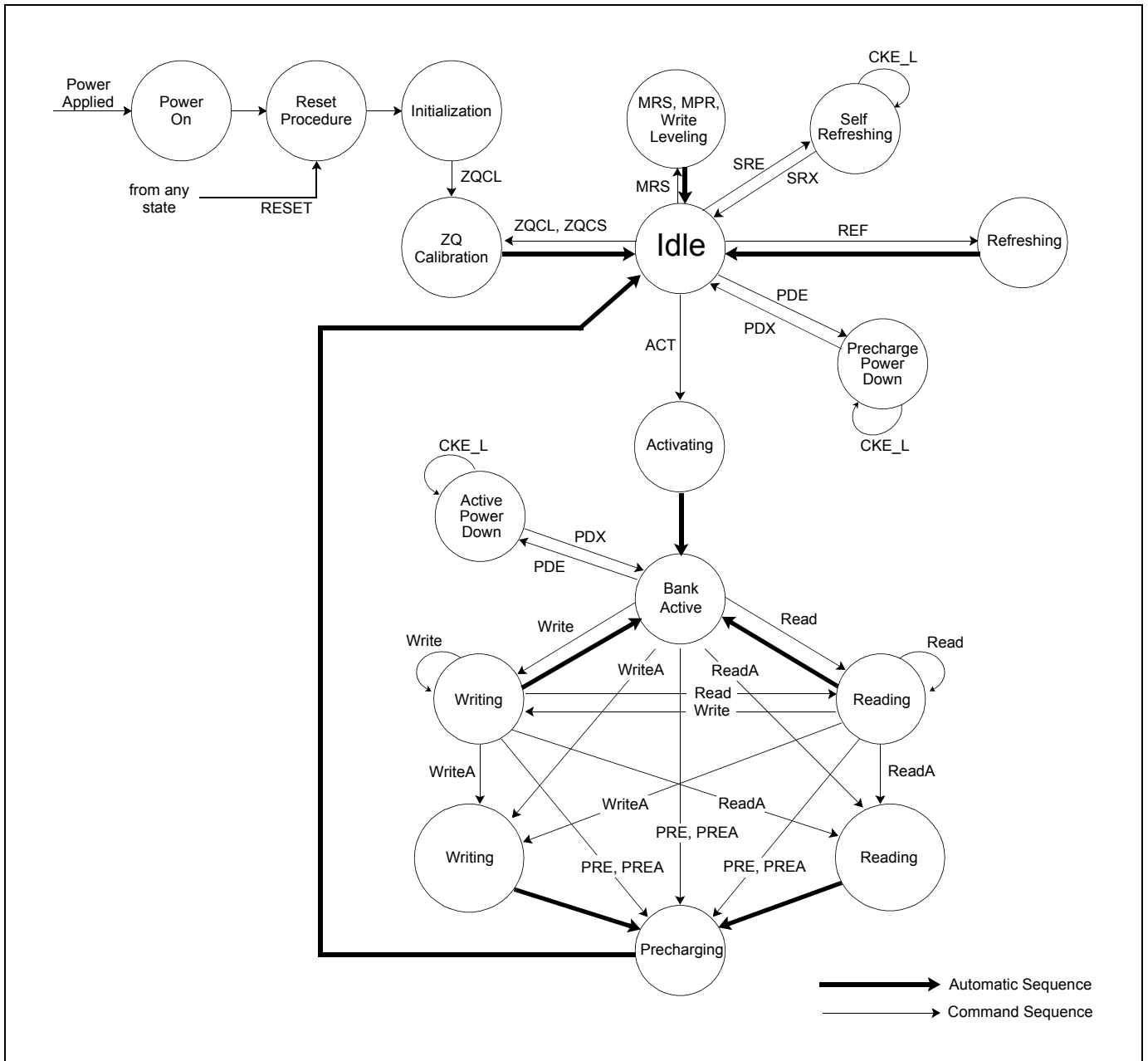


Figure 1. Simplified State Diagram

[Table 1] State Diagram Command Definitions

Abbreviation	Function	Abbreviation	Function	Abbreviation	Function
ACT	Activate	Read	RD,RDS4, RDS8	PDE	Enter Power-down
PRE	Precharge	Read A	RDA,RDAS4, RDAS8	PDX	Exit Power-down
PREA	Precharge All	Write	WR, WRS4, WRS8	SRE	Self-Refresh entry
MRS	Mode Register Set	Write A	WRA,WRAS4, WRAS8	SRX	Self-Refresh exit
REF	Refresh	RESET	Start RESET procedure	MPR	Multi Purpose Register
ZQCL	ZQ Calibration Long	ZQCS	ZQ Calibration Short	-	-

NOTE : This simplified State Diagram is intended to provide an overview of the possible state transitions and the commands to control them. In particular, situations involving more than one bank, the enabling or disabling of on-die termination, and some other events are not captured in full detail.

1.2 Basic Functionality

The DDR3 SDRAM is a high-speed CMOS, dynamic random-access memory internally configured as a eight-bank DRAM. The DDR3 SDRAM uses a 8n prefetch architecture to achieve high-speed operation. The 8n prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR3 SDRAM consists of a single 8n-bit wide, four clock data transfer at the internal DRAM core and two corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins.

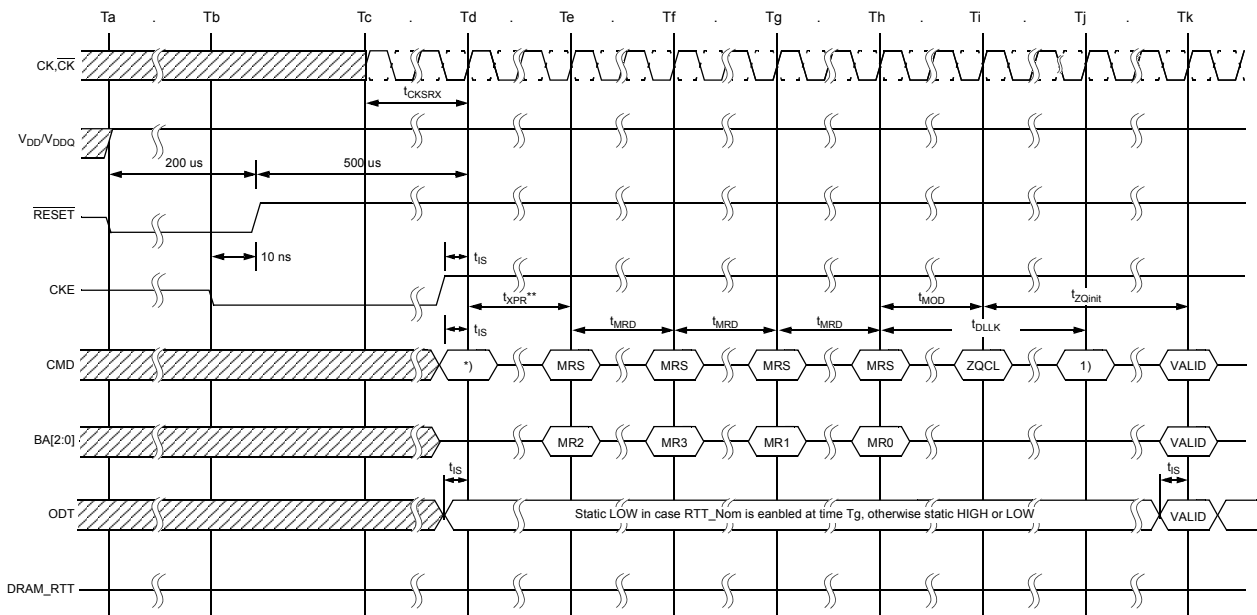
Read and write operation to the DDR3 SDRAM are burst oriented, start at a selected location, and continue for a burst length of four or eight in a programmed sequence. Operation begins with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the Active command are used to select the bank and row to be accessed (BA0-BA2 select the bank; A0-A15 select the row). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst operation, determine if the auto precharge command is to be issued (via A10/AP), and the select BC4 or BL8 mode 'on the fly' (via A12) if enabled in the mode register. Prior to normal operation, the DDR3 SDRAM must be powered up and initialized in a predefined manner. The following sections provide detailed information covering device reset and initialization, register definition, command descriptions and device operation.

1.3 RESET and Initialization Procedure

1.3.1 Power-up Initialization Sequence

The following sequence is required for POWER UP and Initialization.

1. Apply power and attempt to maintain $\overline{\text{RESET}}$ below $0.2 \cdot V_{\text{DD}}$ (all other inputs may be undefined). $\overline{\text{RESET}}$ needs to be maintained for minimum 200us with stable power. CKE is pulled "Low" anytime before $\overline{\text{RESET}}$ being de-asserted (min. time 10ns). The power voltage ramp time between 300mV to V_{DD} min must be no longer than 200ms; and during the ramp, $V_{\text{DD}} > V_{\text{DDQ}}$ and $V_{\text{DD}} - V_{\text{DDQ}} < 0.3$ volts.
 - V_{DD} and V_{DDQ} are driven from a single power converter output, AND
 - The voltage levels on all pins other than $V_{\text{DD}}, V_{\text{DDQ}}, V_{\text{SS}}, V_{\text{SSQ}}$ must be less than or equal to V_{DDQ} and V_{DD} on one side and must be larger than or equal to V_{SSQ} and V_{SS} on the other side. In addition, V_{TT} is limited to 0.95V max once power ramp is finished, AND
 - Vref tracks $V_{\text{DDQ}}/2$.
 - or
 - Apply V_{DD} without any slope reversal before or at the same time as V_{DDQ}
 - Apply V_{DDQ} without any slope reversal before or at the same time as V_{TT} & Vref.
 - The voltage levels on all pins other than $V_{\text{DD}}, V_{\text{DDQ}}, V_{\text{SS}}, V_{\text{SSQ}}$ must be less than or equal to V_{DDQ} and V_{DD} on one side and must be larger than or equal to V_{SSQ} and V_{SS} on the other side.
2. After $\overline{\text{RESET}}$ is de-asserted, wait for another 500us until CKE becomes active. During this time, the DRAM will start internal initialization; this will be done independently of external clocks.
3. Clocks (CK, $\overline{\text{CK}}$) need to be started and stabilized for at least 10ns or 5tCK (which is larger) before CKE goes active. Since CKE is a synchronous signal, the corresponding setup time to clock (tIS) must be met. Also a NOP or Deselect command must be registered (with tIS set up time to clock) before CKE goes active. Once the CKE registered "High" after Reset, CKE needs to be continuously registered "High" until the initialization sequence is finished, including expiration of tDLLK and tZQinit.
4. The DDR3 SDRAM keeps its on-die termination in high-impedance state as long as $\overline{\text{RESET}}$ is asserted. Further, the SDRAM keeps its on-die termination in high impedance state after $\overline{\text{RESET}}$ deassertion until CKE is registered HIGH. The ODT input signal may be in undefined state until tIS before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signal may be statically held at either LOW or HIGH. If RTT_NOM is to be enabled in MR1 and the on-die termination is required to remain in the high impedance state, the ODT input signal must be statically held LOW. In all cases, the ODT input signal remains static until the power up initialization sequence is finished, including the expiration of tDLLK and tZQinit.
5. After CKE is registered high, wait minimum of Reset CKE Exit time, tXPR, before issuing the first MRS command to load mode register. (tXPR=Max(tXS, 5tCK)]
6. Issue MRS Command to load MR2 with all application settings. (To issue MRS command for MR2, provide "Low" to BA0 and BA2, "High" to BA1.)
7. Issue MRS Command to load MR3 with all application settings. (To issue MRS command for MR3, provide "Low" to BA2, "High" to BA0 and BA1.)
8. Issue MRS Command to load MR1 with all application settings and DLL enabled. (To issue "DLL Enable" command, provide "Low" to A0, "Low" to A0, "High" to BA0 and "Low" to BA1-BA2)
9. Issue MRS Command to load MR0 with all application settings and "DLL reset". (To issue DLL reset command, provide "High" to A8 and "Low" to BA0-2).
10. Issue ZQCL command to starting ZQ calibration
11. Wait for both tDLLK and tZQ init completed
12. The DDR3 SDRAM is now ready for normal operation.



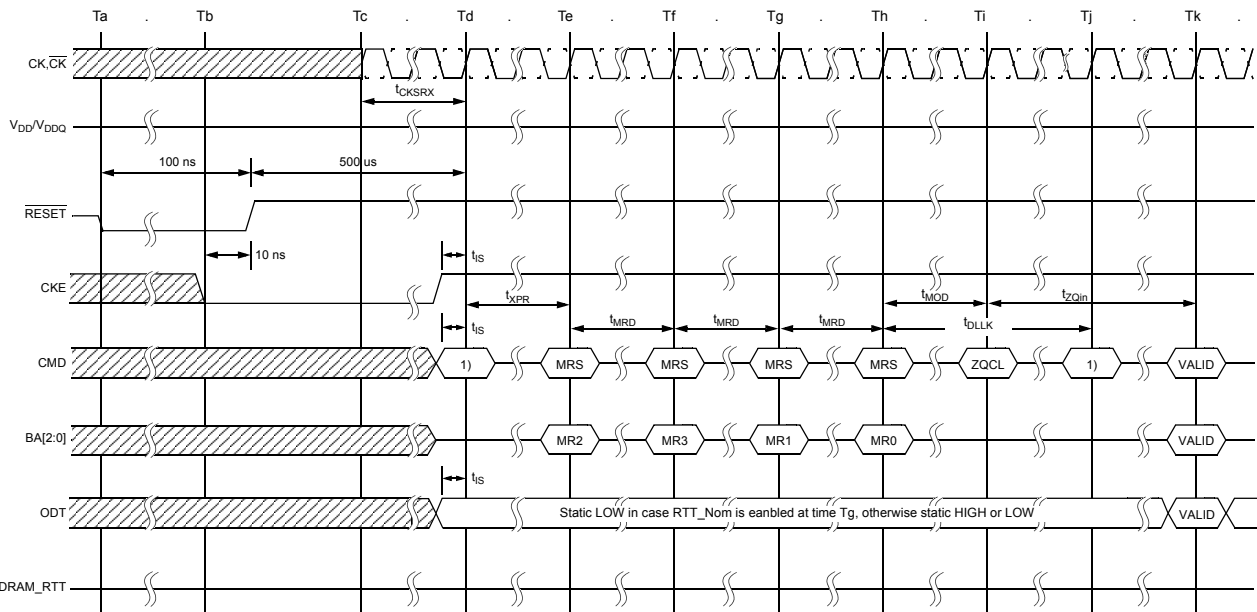
NOTE :
 1) From time point 'Td' until 'Tk', NOP or DES commands must be applied between MRS and ZQCL commands

Figure 2. RESET and Initialization Sequence at Power-on Ramping

1.3.2 Reset Initialization with Stable Power

The following sequence is required for RESET at no power interruption initialization.

1. Asserted RESET below $0.2 \cdot V_{DD}$ anytime when reset is needed (all other inputs may be undefined). RESET needs to be maintained for minimum 100 ns. CKE is pulled "LOW" before RESET being de-asserted (min. time 10 ns).
2. Follow Power-up Initialization Sequence step 2 to 11.
3. The Reset sequence is now completed, DDR3 SDRAM is ready for normal operation.



NOTE :
 1) From time point 'Td' until 'Tk', NOP or DES commands must be applied between MRS and ZQCL commands

Figure 3. RESET procedure at Power stable condition

1.4 Register Definition

1.4.1 Programming the Mode Registers

For application flexibility, various functions, features, and modes are programmable in four Mode Registers, provided by the DDR3 SDRAM, as user defined variables and they must be programmed via a Mode Register Set (MRS) command. As the default values of the Mode Registers (MR#) are not defined, contents of Mode Registers must be fully initialized and/or re-initialized, i.e., written, after power up and/or reset for proper operation. Also the contents of the Mode Registers can be altered by re-executing the MRS command during normal operation. When programming the mode registers, even if the user chooses to modify only a sub-set of the MRS fields, all address fields within the accessed mode register must be redefined when the MRS command is issued. MRS command and DLL Reset do not affect array contents, which means these commands can be executed any time after power-up without affecting the array contents.

The mode register set command cycle time, $tMRD$ is required to complete the write operation to the mode register and is the minimum time required between two MRS commands shown in Figure 4

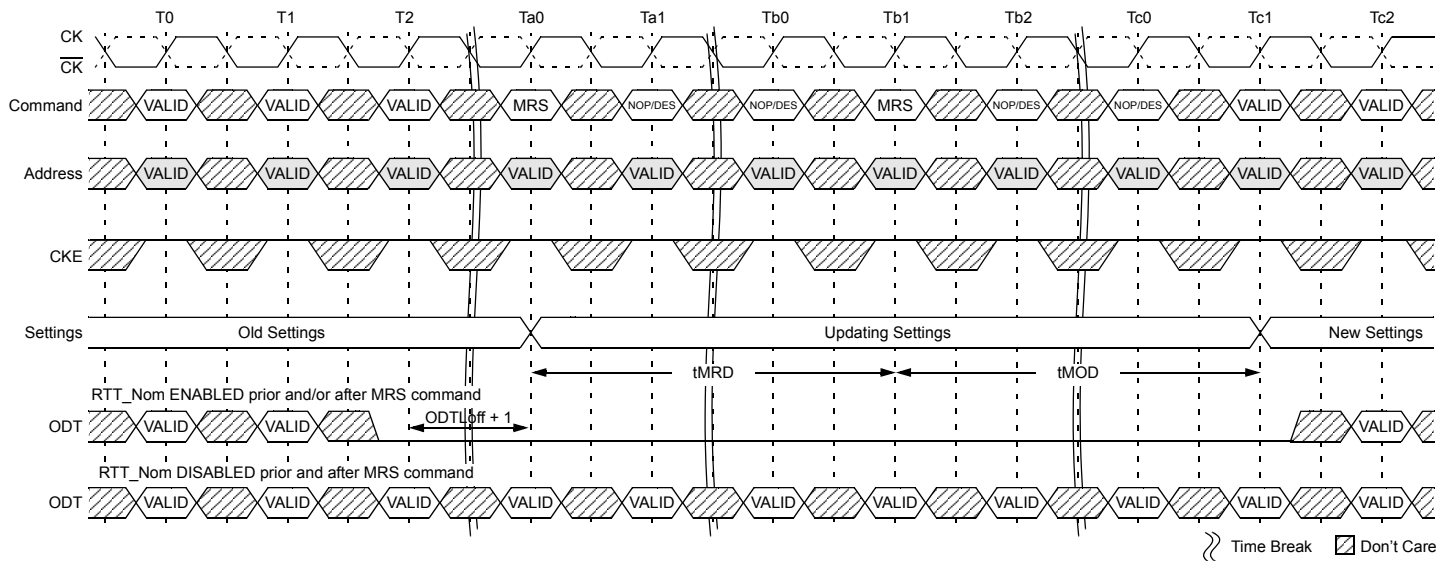


Figure 4. $tMRD$ Timing

The MRS command to Non-MRS command delay, $tMOD$, is required for the DRAM to update the features, except DLL reset, and is the minimum time required from an MRS command to a non-MRS command excluding NOP and DES shown in Figure 5

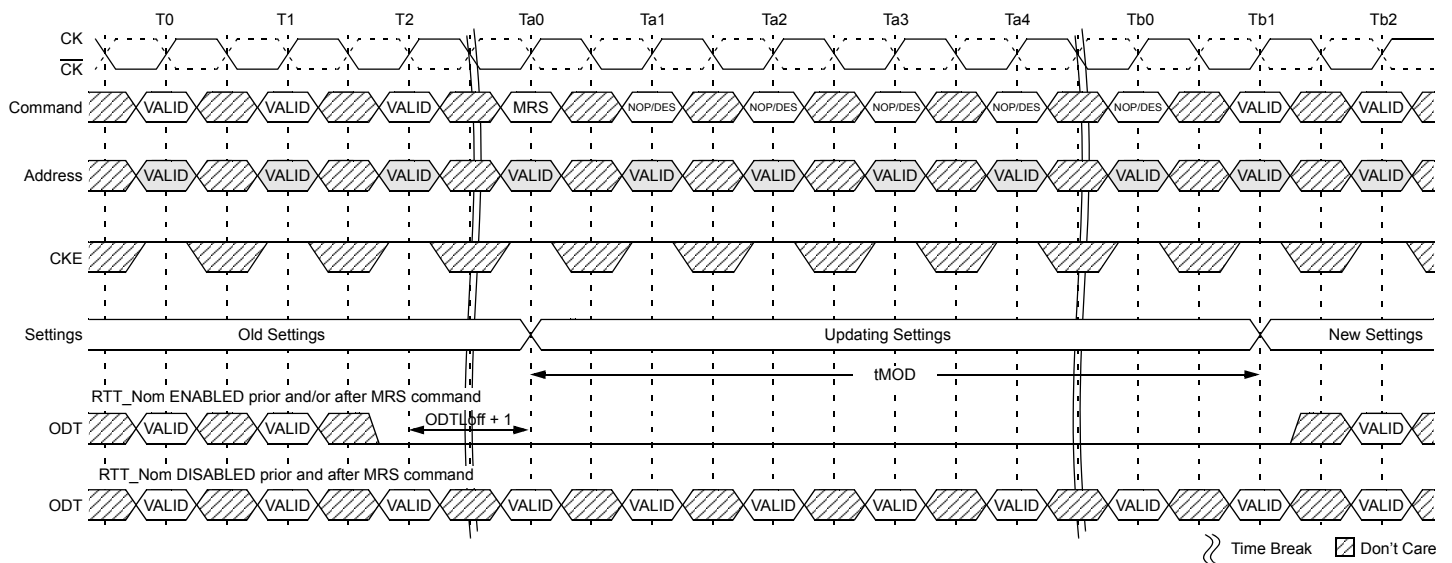


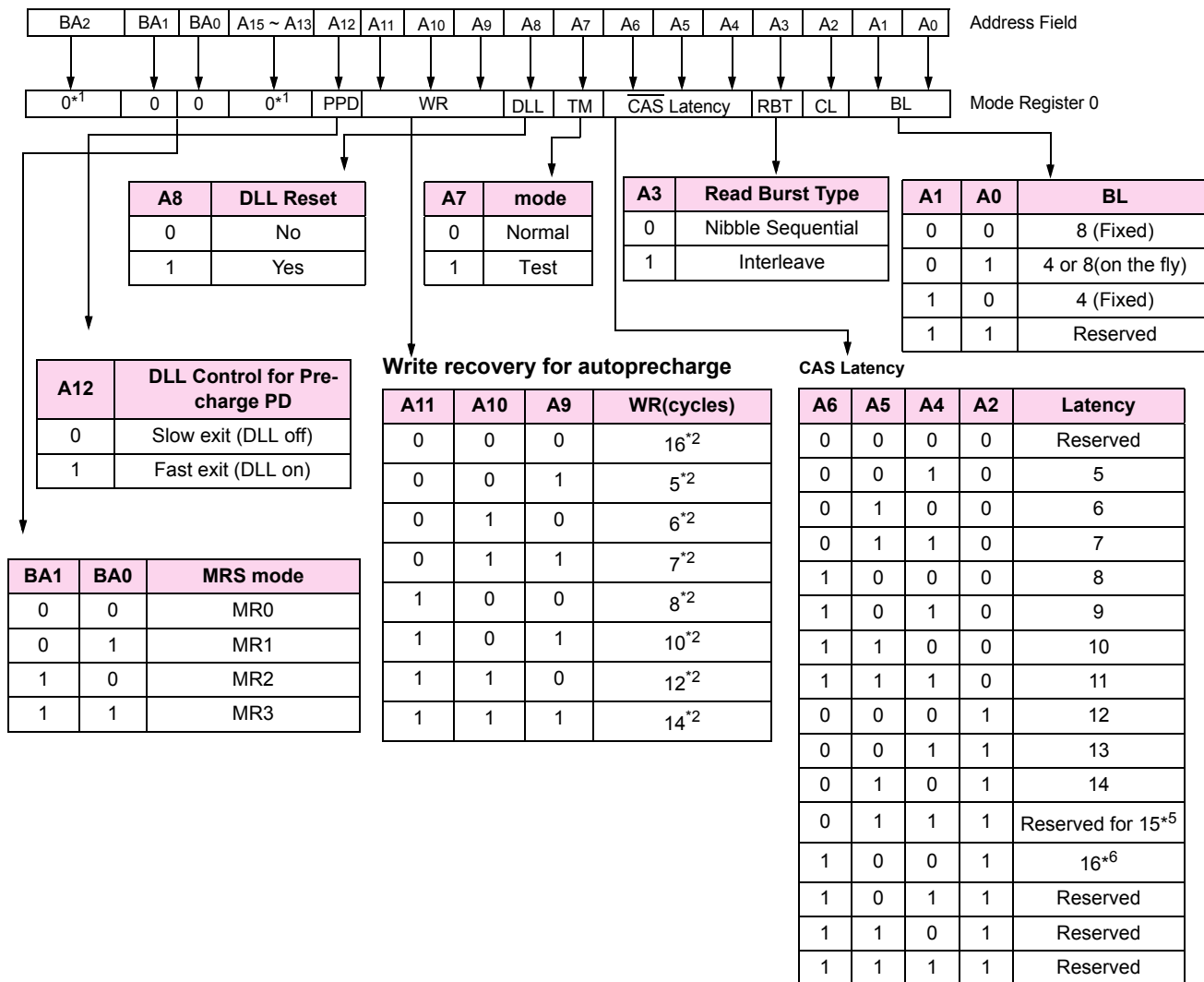
Figure 5. $tMOD$ Timing

1. 4. 2 Programming the Mode Registers (Cont)

The mode register contents can be changed using the same command and timing requirements during normal operation as long as the DRAM is in idle state, i.e., all banks are in the precharged state with tRP satisfied, all data bursts are completed and CKE is high prior to writing into the mode register. If the RTT_NOM feature is enabled in the Mode Register prior and/or after an MRS Command, the ODT Signal must continuously be registered LOW ensuring RTT is in an off State prior to the MRS command. The ODT Signal may be registered high after tMOD has expired. If the RTT_NOM Feature is disabled in the Mode Register prior and after an MRS command, the ODT Signal can be registered either LOW or HIGH before, during and after the MRS command. The mode registers are divided into various fields depending on the functionality and/or modes.

1.4.2 Mode Register MR0

The mode register MR0 stores the data for controlling various operating modes of DDR3 SDRAM. It controls burst length, read burst type, CAS latency, test mode, DLL reset, WR and DLL control for precharge power down, which include various vendor specific options to make DDR3 SDRAM useful for various applications. The mode register is written by asserting low on CS, RAS, CAS, WE, BA0,BA1 and BA2, while controlling the states of address pins according to the Figure below.



NOTE :
 *1 : BA2 and A13~A15 are RFU and must be programmed to 0 during MRS.
 *2 : WR(write recovery for autoprecharge)min in clock cycles is calculated by dividing tWR(in ns) by tCK(in ns) and rounding up to the next integer: $WR_{min}[\text{cycles}] = \text{Roundup}(tWR[\text{ns}]/tCK[\text{ns}])$. The WR value in the mode register must be programmed to be equal or larger than WRmin. The programmed WR value is used with tRP to determine tDAL.
 *3 : The table only shows the encodings for a given Cas Latency. For actual supported Cas Latency, please refer to speedbin tables for each frequency
 *4 : The table only shows the encodings for Write Recovery. For actual Write recovery timing, please refer to AC timingtable
 *5 : RFU(Reserved for Future Use)
 *6 : CL16 is used for gDDR3 1Gb G-die at 2400Mbps operation.

Figure 6. MR0 Definition

1.4.2.1 Burst Length, Type and Order

Accesses within a given burst may be programmed to sequential or interleaved order. The burst type is selected via bit A3 as shown in Figure 6. The ordering of accesses within a burst is determined by the burst length, burst type, and the starting column address as shown in Table 2. The burst length is defined by bits A0-A1. Burst length options include fixed BC4, fixed BL8, and 'on the fly' which allows BC4 or BL8 to be selected coincident with the registration of a Read or Write command via A12/BC.



[Table 2] Burst Type and Burst Order

Burst Length	READ/ WRITE	Starting Column ADDRESS (A2,A1,A0)	burst type = Sequential (decimal) A3 = 0	burst type = Interleaved (decimal) A3 = 1	Notes
4 Chop	READ	0 0 0	0,1,2,3,T,T,T,T	0,1,2,3,T,T,T,T	1, 2, 3
		0 0 1	1,2,3,0,T,T,T,T	1,0,3,2,T,T,T,T	1, 2, 3
		0 1 0	2,3,0,1,T,T,T,T	2,3,0,1,T,T,T,T	1, 2, 3
		0 1 1	3,0,1,2,T,T,T,T	3,2,1,0,T,T,T,T	1, 2, 3
		1 0 0	4,5,6,7,T,T,T,T	4,5,6,7,T,T,T,T	1, 2, 3
		1 0 1	5,6,7,4,T,T,T,T	5,4,7,6,T,T,T,T	1, 2, 3
		1 1 0	6,7,4,5,T,T,T,T	6,7,4,5,T,T,T,T	1, 2, 3
		1 1 1	7,4,5,6,T,T,T,T	7,6,5,4,T,T,T,T	1, 2, 3
	WRITE	0,V,V	0,1,2,3,X,X,X,X	0,1,2,3,X,X,X,X	1, 2, 4, 5
		1,V,V	4,5,6,7,X,X,X,X	4,5,6,7,X,X,X,X	1, 2, 4, 5
8	READ	0 0 0	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7	2
		0 0 1	1,2,3,0,5,6,7,4	1,0,3,2,5,4,7,6	2
		0 1 0	2,3,0,1,6,7,4,5	2,3,0,1,6,7,4,5	2
		0 1 1	3,0,1,2,7,4,5,6	3,2,1,0,7,6,5,4	2
		1 0 0	4,5,6,7,0,1,2,3	4,5,6,7,0,1,2,3	2
		1 0 1	5,6,7,4,1,2,3,0	5,4,7,6,1,0,3,2	2
		1 1 0	6,7,4,5,2,3,0,1	6,7,4,5,2,3,0,1	2
		1 1 1	7,4,5,6,3,0,1,2	7,6,5,4,3,2,1,0	2
	WRITE	V,V,V	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7	2, 4

NOTE :

- In case of burst length being fixed to 4 by MR0 setting, the internal write operation starts two clock cycles earlier than for the BL8 mode. This means that the starting point for tWR and tWTR will be pulled in by two clocks. In case of burst length being selected on-the-fly via A12/BC, the internal write operation starts at the same point in time like a burst of 8 write operation. This means that during on-the-fly control, the starting point for tWR and tWTR will not be pulled in by two clocks.
- 0...7 bit number is value of CA[2:0] that causes this bit to be the first read during a burst.
- T: Output driver for data and strobes are in high impedance.
- V: a valid logic level (0 or 1), but respective buffer input ignores level on input pins.
- X: Don't Care.

1.4.2.2 CAS Latency

The CAS Latency is defined by MR0(bits A4-A6) as shown in Figure 6. CAS Latency is the delay, in clock cycles, between the internal Read command and the availability of the first bit of output data. DDR3 SDRAM does not support any half clock latencies. The overall Read Latency (RL) is defined as Additive Latency (AL) + CAS Latency (CL); $RL = AL + CL$. For more information on the supported CL and AL settings based on the operating clock frequency, refer to "Standard Speed Bins" on each component datasheet. For detailed Read operation refer to "READ Operation" on page 30

1.4.2.3 Test Mode

The normal operating mode is selected by MR0(bit A7 = 0) and all other bits set to the desired values shown in Figure 6. Programming bit A7 to a '1' places the DDR3 SDRAM into a test mode that is only used by the DRAM Manufacturer and should NOT be used. No operations or functionality is guaranteed if A7 = 1.

1.4.2.4 DLL Reset

The DLL Reset bit is self-clearing, meaning it returns back to the value of '0' after the DLL reset function has been issued. Once the DLL is enabled, a subsequent DLL Reset should be applied. Any time the DLL reset function is used, tDLLK must be met before any functions that require the DLL can be used (i.e. Read commands or ODT synchronous operations).

1.4.2.5 Write Recovery

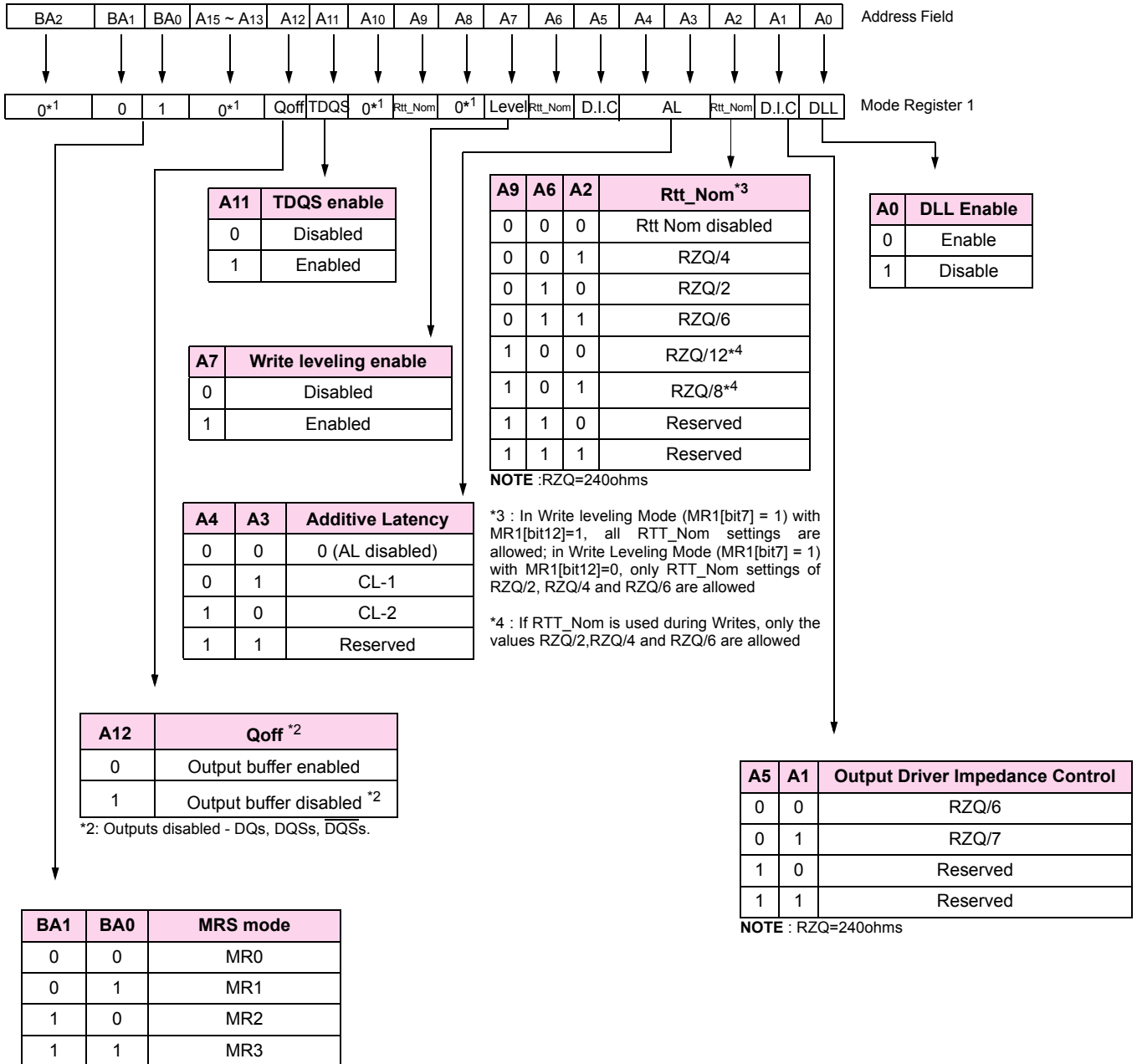
The programmed WR value MR0(bits A9, A10, and A11) is used for the auto precharge feature along with tRP to determine tDAL WR(write recovery for auto-precharge)min in clock cycles is calculated by dividing tWR(in ns) by tCK(in ns) and rounding up to the next integer: $WR_{min}[\text{cycles}] = \text{Roundup}(tWR[\text{ns}]/tCK[\text{ns}])$. The WR must be programmed to be equal or larger than tWR(min).

1.4.2.6 Precharge PD DLL

MR0 (bit A12) is used to select the DLL usage during precharge power-down mode. When MR0(A12 = 0), or "slow-exit", the DLL is frozen after entering precharge power-down (for potential power savings) and upon exit requires tXPDLL to be met prior to the next valid command. When MR0(A12 = 1), or "fast-exit", the DLL is maintained after entering precharge power-down and upon exiting power-down requires tXP to be met prior to the next valid command.

1.4.3 Mode Register MR1

The Mode Register MR1 stores the data for enabling or disabling the DLL, output driver strength, Rtt_Nom impedance, additive latency, Write leveling enable, TDQS enable and Qoff. The Mode Register 1 is written by asserting low on CS, RAS, CAS, WE, high on BA0 and low on BA1 and BA2 while controlling the states of address pins according to the Figure below.



* 1 : BA2 and A8, A10 and A13 ~ A15 are RFU and must be programmed to 0 during MRS

Figure 7. MR1 Definition

1.4.3.1 DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power up initialization, and upon returning to normal operation after having the DLL disabled. During normal operation (DLL-on) with MR1(A0 = 0), the DLL is automatically disabled when entering Self-Refresh operation and is automatically re-enabled upon exit of Self-Refresh operation. Any time the DLL is enabled and subsequently reset, tDLLK clock cycles must occur before a Read or synchronous ODT command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the tDQSCK, tAON or tAOF parameters. During tDLLK, CKE must continuously be registered high. DDR3 SDRAM does not require DLL for any Write operation. For more detailed information on DLL Disable operation refer to "DLL-off Mode" on page 18

The direct ODT feature is not supported during DLL-off mode. The on-die termination resistors must be disabled by continuously registering the ODT pin low and/or by programming the RTT_Nom bits MR1{A9,A6,A2} to {0,0,0} via a mode register set command during DLL-off mode.

The dynamic ODT feature is not supported at DLL-off mode. User must use MRS command to set Rtt_WR, MR2{A10, A9}={0,0}, to disable Dynamic ODT externally.

1.4.3.2 Output Driver Impedance Control

The output driver impedance of the DDR3 SDRAM device is selected by MR1(bits A1 and A5) as shown in Figure 7

1.4.3.3 ODT Rtt Values

DDR3 SDRAM is capable of providing two different termination values (Rtt_Nom and Rtt_WR). The nominal termination value Rtt_Nom is programmed in MR1. A separate value (Rtt_WR) may be programmed in MR2 to enable a unique RTT value when ODT is enabled during writes. The Rtt_WR value can be applied during writes even when Rtt_Nom is disabled.

1.4.3.4 Additive Latency (AL)

Additive Latency (AL) operation is supported to make command and data bus efficient for sustainable bandwidths in DDR3 SDRAM. In this operation, the DDR3 SDRAM allows a read or write command (either with or without auto-precharge) to be issued immediately after the active command. The command is held for the time of the Additive Latency (AL) before it is issued inside the device. The Read Latency (RL) is controlled by the sum of the AL and CAS Latency (CL) register settings. Write Latency (WL) is controlled by the sum of the AL and CAS Write Latency (CWL) register settings. A summary of the AL register options are shown in Table 3

[Table 3] Additive Latency (AL) Settings

A4	A3	AL
0	0	0 (AL Disabled)
0	1	CL - 1
1	0	CL - 2
1	1	Reserved

NOTE : AL has a value of CL - 1 or CL - 2 as per the CL values programmed in the MR0 register.

1.4.3.5 Write leveling

For better signal integrity, DDR3 memory module adopted fly by topology for the commands, addresses, control signals and clocks. The fly by topology has benefits from reducing number of stubs and their length but in other aspect, causes flight time skew between clock and strobe at every DRAM on DIMM. It makes it difficult for the Controller to maintain tDQSS, tDSS and tDSH specification. Therefore, the DDR3 SDRAM supports 'write leveling' feature to allow the controller to compensate for skew. See "Write Leveling" on page 22. for more details.

1.4.3.6 Output Disable

The DDR3 SDRAM outputs may be enabled/disabled by MR1(bit A12) as shown in Figure 7. When this feature is enabled (A12 = 1), all output pins (DQs, DQS, DQS, etc.) are disconnected from the device removing any loading of the output drivers. This feature may be useful when measuring module power for example. For normal operation, A12 should be set to '0'.

1.4.3.7 TDQS, $\overline{\text{TDQS}}$

TDQS (Termination Data Strobe) is a feature of X8 DDR3 SDRAM that provides additional termination resistance outputs that may be useful in some system configurations.

TDQS is not supported in X4 or X16 configurations. When enabled via the mode register, the same termination resistance function is applied to the TDQS/ $\overline{\text{TDQS}}$ pins that is applied to the DQS/ $\overline{\text{DQS}}$ pins.

In contrast to the RDQS function of DDR2 SDRAM, TDQS provides the termination resistance function only. The data strobe function of RDQS is not provided by TDQS.

The TDQS and DM functions share the same pin. When the TDQS function is enabled via the mode register, the DM function is not supported. When the TDQS function is disabled, the DM function is provided and the $\overline{\text{TDQS}}$ pin is not used. Table 4 for details.

The TDQS function is available in X8 DDR3 SDRAM only and must be disabled via the mode register A11=0 in MR1 for X4 and X16 configurations.

[Table 4] TDQS, $\overline{\text{TDQS}}$ Function Matrix

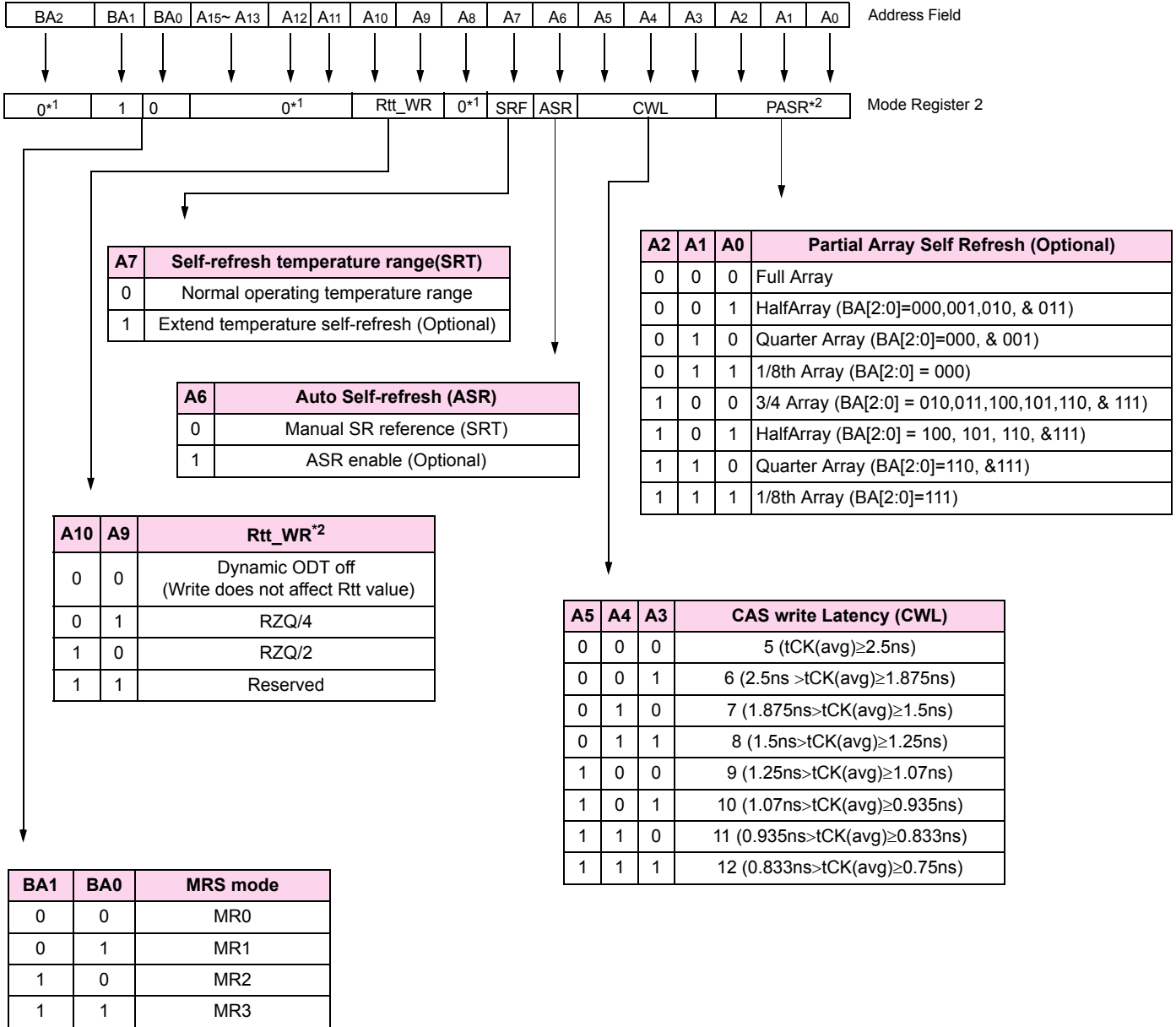
MR1(A11)	DM / TDQS	NU / $\overline{\text{TDQS}}$
0 (TDQS Disabled)	DM	Hi-Z
1 (TDQS Enabled)	TDQS	$\overline{\text{TDQS}}$

NOTE :

1. If TDQS is enabled, the DM function is disabled.
2. When not used, TDQS function can be disabled to save termination power.
3. TDQS function is only available for x8 DRAM and must be disabled for x4 and x16.

1.4.4 Mode Register MR2

The Mode Register MR2 stores the data for controlling refresh related features, Rtt_WR impedance, and CAS write latency. The Mode Register 2 is written by asserting low on CS, RAS, CAS, WE, high on BA1 and low on BA0 and BA2, while controlling the states of address pins according to the table below.



* 1 : BA2, A5, A8, A11 ~ A15 are RFU and must be programmed to 0 during MRS.
 * 2 : The Rtt_WR value can be applied during writes even when Rtt_Nom is disabled.
 During write leveling, Dynamic ODT is not available.

Figure 8. MR2 Definition

1.4.4.1 Partial Array Self-Refresh (PASR)

Optional in DDR3 SDRAM: Users should refer to the DRAM component data sheet and/or the DIMM SPD to determine if DDR3 SDRAM devices support the following options or requirements referred to in this material. If PASR (Partial Array Self-Refresh) is enabled, data located in areas of the array beyond the specified address range shown in Figure 8 will be lost if Self-Refresh is entered. Data integrity will be maintained if tREFI conditions are met and no Self-Refresh command is issued.

1.4.4.2 CAS Write Latency (CWL)

The CAS Write Latency is defined by MR2 (bits A3-A5), as shown in Figure 8. CAS Write Latency is the delay, in clock cycles, between the internal Write command and the availability of the first bit of input data. DDR3 SDRAM does not support any half clock latencies. The overall Write Latency (WL) is defined as Additive Latency (AL) + CAS Write Latency (CWL); $WL = AL + CWL$. For more information on the supported CWL and AL settings based on the operating clock frequency, refer to "Standard Speed Bins" on each component datasheet. For detailed Write operation refer to "WRITE Operation" on page 41

1.4.4.3 Auto Self-Refresh (ASR) and Self-Refresh Temperature (SRT)

Optional in DDR3 SDRAM: Users should refer to the DRAM component data sheet and/or the DIMM SPD to determine if DDR3 SDRAM devices support the following options or requirements referred to in this material. For more details refer to 'Extended Temperature Usage' DDR3 SDRAM's must support Self-Refresh operation at all supported temperatures. Applications requiring Self-Refresh operation in the Extended Temperature Range must use the optional ASR function or program the SRT bit appropriately.

1.4.4.4 Dynamic ODT (Rtt_WR)

DDR3 SDRAM introduces a new feature "Dynamic ODT". In certain application cases and to further enhance signal integrity on the data bus, it is desirable that the termination strength of the DDR3 SDRAM can be changed without issuing an MRS command. MR2 Register locations A9 and A10 configure the Dynamic ODT settings. In Write leveling mode, only RTT_Nom is available. For details on ODT operation, refer to "Dynamic ODT" on page 62.

1.4.5 Mode Register MR3

The Mode Register MR3 controls Multi purpose registers. The Mode Register 3 is written by asserting low on \overline{CS} , \overline{RAS} , \overline{CAS} , \overline{WE} , high on BA1 and BA0, while controlling the states of address pins according to the table below.

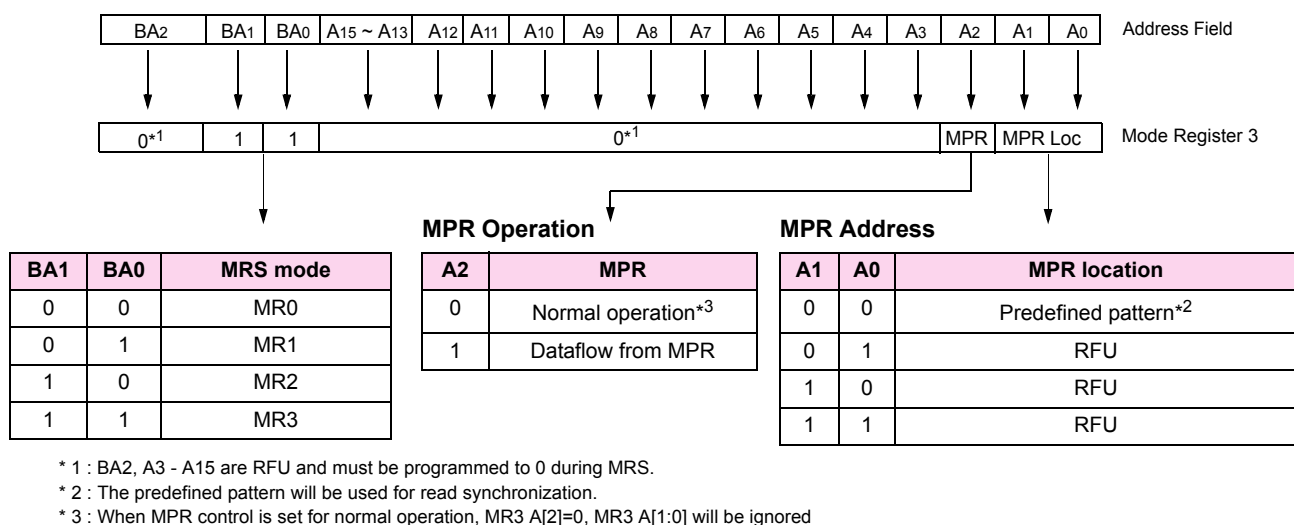


Figure 9. MR3 Definition

1.4.5.1 Multi-Purpose Register (MPR)

The Multi Purpose Register (MPR) function is used to Read out a predefined system timing calibration bit sequence. To enable the MPR, a MODE Register Set (MRS) command must be issued to MR3 Register with bit A2 = 1. Prior to issuing the MRS command, all banks must be in the idle state (all banks precharged and tRP/tRPA met). Once the MPR is enabled, any subsequent RD or RDA commands will be redirected to the Multi Purpose Register. When the MPR is enabled, only RD or RDA commands are allowed until a subsequent MRS command is issued with the MPR disabled (MR3 bit A2 = 0). Power-Down mode, Self-Refresh, and any other non-RD/RDA command is not allowed during MPR enable mode. The RESET function is supported during MPR enable mode. For detailed MPR operation refer to "Multi Purpose Register" on page 26.

2. DDR3 SDRAM Command Description and Operation

2.1 Command Truth Table

a) Note 1,2,3 and 4 apply to the entire Command truth table

(b) Note 5 applies to all Read/Write commands.

[BA=Bank Address, RA=Row Address, CA=Column Address, \overline{BC} =Burst Chop, X=Don't care, V=Valid]

[Table 5] Command Truth Table

Function	Abbreviation	CKE		\overline{CS}	\overline{RAS}	\overline{CAS}	\overline{WE}	BA0 - BA2	A13 - A15	A12 / \overline{BC}	A10 / AP	A0 - A9,A11	NOTE
		Previous Cycle	Current Cycle										
Mode Register Set	MRS	H	H	L	L	L	L	BA	OP Code				
Refresh	REF	H	H	L	L	L	H	V	V	V	V	V	
Self Refresh Entry	SRE	H	L	L	L	L	H	V	V	V	V	V	7,9,12
Self Refresh Exit	SRX	L	H	H	V	V	V	X	X	X	X	X	7,8,9,12
				L	H	H	H	V	V	V	V	V	
Single Bank Precharge	PRE	H	H	L	L	H	L	BA	V	V	L	V	
Precharge all Banks	PREA	H	H	L	L	H	L	V	V	V	H	V	
Bank Activate	ACT	H	H	L	L	H	H	BA	Row Address (RA)				
Write (Fixed BL8 or BL4)	WR	H	H	L	H	L	L	BA	RFU	V	L	CA	
Write (BL4, on the Fly)	WRS4	H	H	L	H	L	L	BA	RFU	L	L	CA	
Write (BL8, on the Fly)	WRS8	H	H	L	H	L	L	BA	RFU	H	L	CA	
Write with Auto Precharge (Fixed BL8 or BL4)	WRA	H	H	L	H	L	L	BA	RFU	V	H	CA	
Write with Auto Precharge (BL4, on the Fly)	WRAS4	H	H	L	H	L	L	BA	RFU	L	H	CA	
Write with Auto Precharge (BL8, on the Fly)	WRAS8	H	H	L	H	L	L	BA	RFU	H	H	CA	
Read (Fixed BL8 or BL4)	RD	H	H	L	H	L	H	BA	RFU	V	L	CA	
Read (BL4, on the Fly)	RDS4	H	H	L	H	L	H	BA	RFU	L	L	CA	
Read (BL8, on the Fly)	RDS8	H	H	L	H	L	H	BA	RFU	H	L	CA	
Read with Auto Precharge (Fixed BL8 or BL4)	RDA	H	H	L	H	L	H	BA	RFU	V	H	CA	
Read with Auto Precharge (BL4, on the Fly)	RDAS4	H	H	L	H	L	H	BA	RFU	L	H	CA	
Read with Auto Precharge (BL8, on the Fly)	RDAS8	H	H	L	H	L	H	BA	RFU	H	H	CA	
No Operation	NOP	H	H	L	H	H	H	V	V	V	V	V	10
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	11
ZQ calibration Long	ZQCL	H	H	L	H	H	L	X	X	X	H	X	
ZQ calibration Short	ZQCS	H	H	L	H	H	L	X	X	X	L	X	
Power Down Entry	PDE	H	L	L	H	H	H	V	V	V	V	V	6,12
				H	V	X	X	X	X	X	X	X	
Power Down Exit	PDX	L	H	L	H	H	H	V	V	V	V	V	6,12
				H	X	X	X	X	X	X	X	X	

NOTE :

- All DDR3 SDRAM commands are defined by states of \overline{CS} , \overline{RAS} , \overline{CAS} , \overline{WE} and CKE at the rising edge of the clock. The MSB of BA, RA, and CA are device density and configuration dependant
- \overline{RESET} is Low enable command which will be used only for asynchronous reset so must be maintained HIGH during any function.
- Bank addresses (BA) determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register
- "V" means "H or L (but a defined logic level)" and "X" means either "defined or undefined (like floating) logic level"
- Burst reads or writes cannot be terminated or interrupted and Fixed/on the fly BL will be defined by MRS
- The Power Down Mode does not perform any refresh operations.
- The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
- Self refresh exit is asynchronous.
- V_{REF} (Both V_{REFDQ} and V_{REFCA}) must be maintained during Self Refresh operation. V_{refDQ} supply can be turned OFF in system during Self Refresh operation, provided that V_{refDQ} is valid and stable prior to CKE going back High and that first Write operation may not occur earlier than 512nCK after exit from Self Refresh.
- The No Operation command should be used in cases when the DDR3 SDRAM is in an idle or a wait state. The purpose of the No Operation command (NOP) is to prevent the DDR3 SDRAM from registering any unwanted commands between operations. A No Operation command will not terminate a previous operation that is still executing, such as a burst read or write cycle.
- The Deselect command performs the same function as a No Operation command.
- Refer to the CKE Truth Table for more detail with CKE transition

2.2 Clock Enable (CKE) Truth Table

- (a) Note 1~7 apply to the entire Command truth table
 (b) For Power-down entry and exit parameters See 2.17, [?\\$paratext>,?](#) on page 51
 (c) CKE low is allowed only if tMRD and tMOD are satisfied

[Table 6] CKE Truth Table

Current State ²	CKE		Command (N) ³ $\overline{\text{RAS}}, \overline{\text{CAS}}, \overline{\text{WE}}, \overline{\text{CS}}$	Action (N) ³	NOTE
	Previous Cycle ¹ (N-1)	Current Cycle ¹ (N)			
Power Down	L	L	X	Maintain Power-Down	14, 15
	L	H	DESELECT or NOP	Power Down Exit	11, 14
Self Refresh	L	L	X	Maintain Self Refresh	15, 16
	L	H	DESELECT or NOP	Self Refresh Exit	8, 12, 16
Bank(s) Active	H	L	DESELECT or NOP	Active Power Down Entry	11, 13, 14
Reading	H	L	DESELECT or NOP	Power Down Entry	11, 13, 14, 17
Writing	H	L	DESELECT or NOP	Power Down Entry	11, 13, 14, 17
Precharging	H	L	DESELECT or NOP	Power Down Entry	11, 13, 14, 17
Refreshing	H	L	DESELECT or NOP	Precharge Power Down Entry	11
All Banks Idle	H	L	DESELECT or NOP	Precharge Power Down Entry	11,13, 14, 18
	H	L	REFRESH	Self Refresh Entry	9, 13, 18
For more details with all signals See Table 5 "Command Truth Table" on page 16					10

NOTE :

- CKE (N) is the logic state of CKE at clock edge N; CKE (N-1) was the state of CKE at the previous clock edge.
- Current state is defined as the state of the DDR3 SDRAM immediately prior to clock edge N
- COMMAND (N) is the command registered at clock edge N, and ACTION (N) is a result of COMMAND (N), ODT is not included here
- All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document
- The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh
- CKE must be registered with the same value on tCKEmin consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the tCKEmin clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of tIS + tCKEmin + tIH.
- DESELECT and NOP are defined in the Command truth table
- On Self Refresh Exit DESELECT or NOP commands must be issued on every clock edge occurring during the tXS period. Read or ODT commands may be issued only after tXSDLL is satisfied.
- Self Refresh mode can only be entered from the All Banks Idle state.
- Must be a legal command as defined in the Command Truth Table.
- Valid commands for Power Down Entry and Exit are NOP and DESELECT only.
- Valid commands for Self Refresh Exit are NOP and DESELECT only.
- Self Refresh can not be entered while Read or Write operations. See Figure 2.16 and Figure 2.17 for a detailed list of restrictions.
- The Power Down does not perform any refresh operations.
- "X" means "don't care (including floating around V_{REF})" in Self Refresh and Power Down. It also applies to Address pins
- V_{REF} (Both V_{REFDQ} and V_{REFCA}) must be maintained during Self Refresh operation. VrefDQ supply may be turned OFF in system during Self Refresh operation, provided that VrefDQ is valid and stable prior to CKE going back High and that first Write operation may not occur earlier than 512nCK after exit from Self Refresh.
- If all banks are closed at the conclusion of the read, write or precharge command, then Precharge Power Down is entered, otherwise Active Power Down is entered
- 'Idle state' means that all banks are closed (tRP, tDAL, etc. satisfied) and CKE is high and all timings from previous operations are satisfied (tMRD, tMOD, tRFC, tZQinit, tZQoper, tZQCS, etc) as well as all SRF exit and Power Down exit parameters are satisfied (tXS, tXP, tXPDLL, etc)

2.3 No Operation (NOP) Command

The No Operation (NOP) command is used to instruct the selected DDR3 SDRAM to perform a NOP ($\overline{\text{CS}}$ LOW and $\overline{\text{RAS}}, \overline{\text{CAS}},$ and $\overline{\text{WE}}$ HIGH). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

2.4 Deselect Command

The DESELECT function ($\overline{\text{CS}}$ HIGH) prevents new commands from being executed by the DDR3 SDRAM. The DDR3 SDRAM is effectively deselected. Operations already in progress are not affected.

2.5 DLL-off Mode

DDR3 DLL-off mode is entered by setting MR1 bit A0 to "1"; this will disable the DLL for subsequent operations until A0 bit set back to "0". The MR1 A0 bit for DLL control can be switched either during initialization or later. Refer to "Input clock frequency change" on page 21.

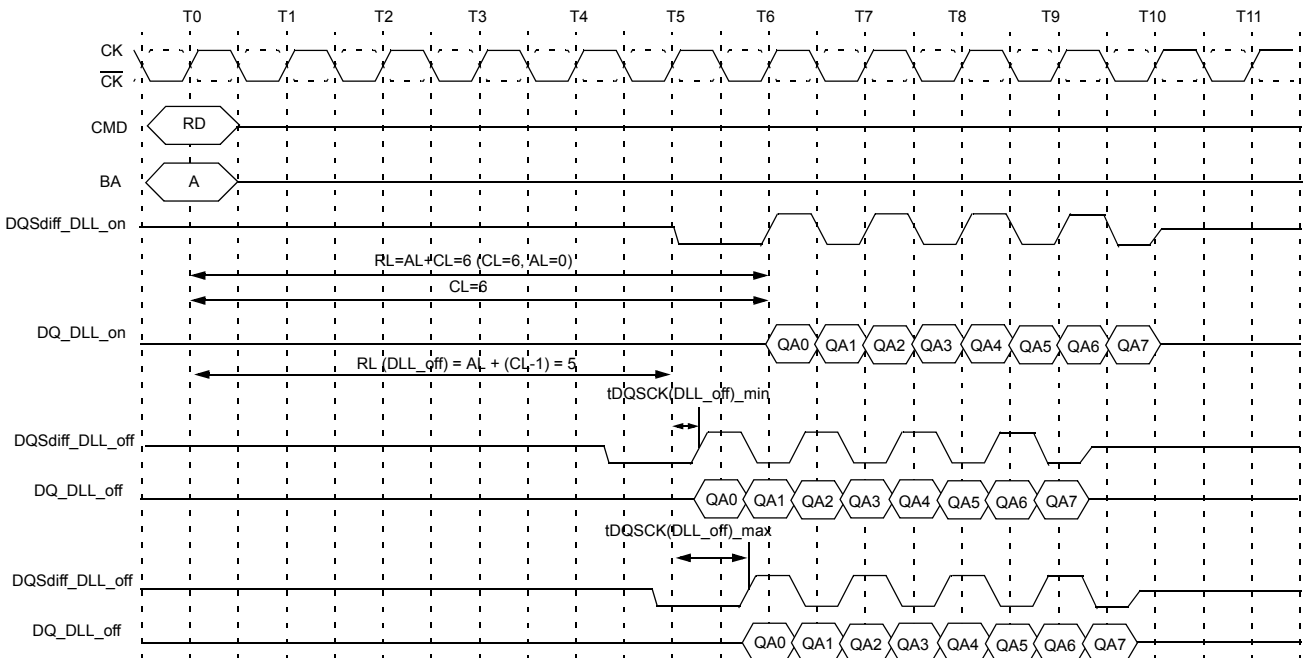
The DLL-off Mode operations listed below are an optional feature for DDR3. The maximum clock frequency for DLL-off Mode is specified by the parameter tCKDLL-OFF. There is no minimum frequency limit besides the need to satisfy the refresh interval, tREFI.

Due to latency counter and timing restrictions, only one value of CAS Latency (CL) in MR0 and CAS Write Latency (CWL) in MR2 are supported. The DLL-off mode is only required to support setting of both CL=6 and CWL=6.

DLL-off mode will affect the Read data Clock to Data Strobe relationship (tDQSCK), but not the Data Strobe to Data relationship (tDQSQ, tQH). Special attention is needed to line up Read data to controller time domain.

Comparing with DLL-on mode, where tDQSCK starts from the rising clock edge (AL+CL) cycles after the Read command, the DLL-off mode tDQSCK starts (AL+CL - 1) cycles after the read command. Another difference is that tDQSCK may not be small compared to tCK (it might even be larger than tCK) and the difference between tDQSCKmin and tDQSCKmax is significantly larger than in DLL-on mode.

The timing relations on DLL-off mode READ operation have shown at following Timing Diagram (CL=6, BL=8):



NOTE : The tDQSCK is used here for DQS, \overline{DQS} and DQ to have a simplified diagram; the DLL_off shift will affect both timings in the same way and the skew between all DQ and DQS, DQS signals will still be tDQSQ.

Figure 10. DLL-off mode READ Timing Operation

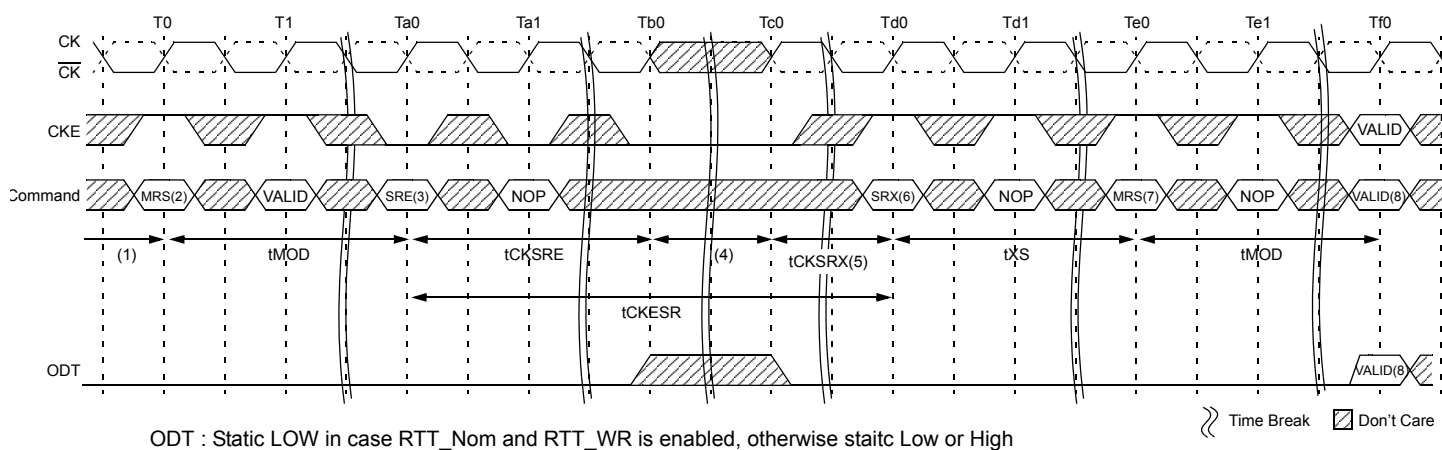
2.6 DLL on/off switching procedure

DDR3 DLL-off mode is entered by setting MR1 bit A0 to "1"; this will disable the DLL for subsequent operations until A0 bit set back to "0".

2.6.1 DLL "on" to DLL "off" Procedure

To switch from DLL "on" to DLL "off" requires the frequency to be changed during Self-Refresh outlined in the following procedure:

1. Starting from Idle state (All banks pre-charged, all timings fulfilled, and DRAMs On-die Termination resistors, RTT, must be in high impedance state before MRS to MR1 to disable the DLL.)
2. Set MR1 bit A0 to "1" to disable the DLL.
3. Wait tMOD.
4. Enter Self Refresh Mode; wait until (tCKSRE) is satisfied.
5. Change frequency, in guidance with "Input clock frequency change" on page 21
6. Wait until a stable clock is available for at least (tCKSRX) at DRAM inputs.
7. Starting with the Self Refresh Exit command, CKE must continuously be registered HIGH until all tMOD timings from any MRS command are satisfied. In addition, if any ODT features were enabled in the mode registers when Self Refresh mode was entered, the ODT signal must continuously be registered LOW until all tMOD timings from any MRS command are satisfied. If both ODT features were disabled in the mode registers when Self Refresh mode was entered, ODT signal can be registered LOW or HIGH.
8. Wait tXS, then set Mode Registers with appropriate values (especially an update of CL, CWL and WR may be necessary. A ZQCL command may also be issued after tXS)
9. Wait for tMOD, then DRAM is ready for next command.



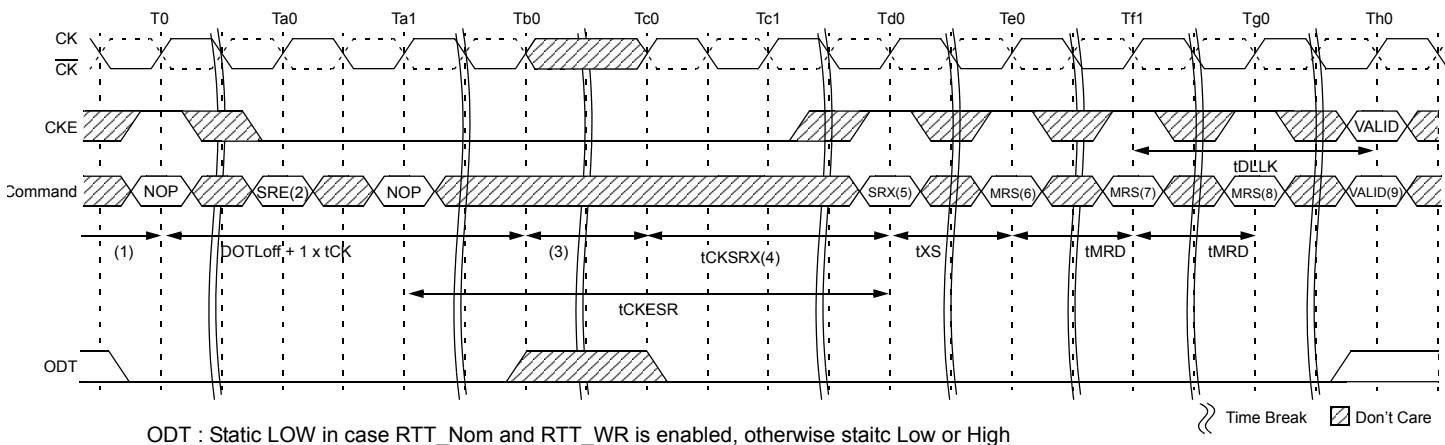
- NOTE :**
1. Starting with Idle State, RTT in Hi-Z state
 2. Disable DLL by setting MR1 Bit A0 to 1
 3. Enter SR
 4. Change Frequency
 5. Clock must be stable tCKSRX
 6. Exit SR
 7. Update Mode registers with DLL off parameters setting
 8. Any valid command

Figure 11. DLL Switch Sequence from DLL-on to DLL-off

2.6.2 DLL "off" to DLL "on" Procedure

To switch from DLL "off" to DLL "on" (with required frequency change) during Self-Refresh:

1. Starting from Idle state (All banks pre-charged, all timings fulfilled and DRAMs On-die Termination resistors (RTT) must be in high impedance state before Self-Refresh mode is entered.)
2. Enter Self Refresh Mode, wait until tCKSRE satisfied.
3. Change frequency, in guidance with "Input clock frequency change" on page 21
4. Wait until a stable clock is available for at least (tCKSRX) at DRAM inputs.
5. Starting with the Self Refresh Exit command, CKE must continuously be registered HIGH until tDLLK timing from subsequent DLL Reset command is satisfied. In addition, if any ODT features were enabled in the mode registers when Self Refresh mode was entered, the ODT signal must continuously be registered LOW until tDLLK timings from subsequent DLL Reset command is satisfied. If both ODT features are disabled in the mode registers when Self Refresh mode was entered, ODT signal can be registered LOW or HIGH.
6. Wait tXS, then set MR1 bit A0 to "0" to enable the DLL.
7. Wait tMRD, then set MR0 bit A8 to "1" to start DLL Reset.
8. Wait tMRD, then set Mode Registers with appropriate values (especially an update of CL, CWL and WR may be necessary. After tMOD satisfied from any proceeding MRS command, a ZQCL command may also be issued during or after tDLLK.)
9. Wait for tMOD, then DRAM is ready for next command (Remember to wait tDLLK after DLL Reset before applying command requiring a locked DLL!). In addition, wait also for tZQoper in case a ZQCL command was issued.



- NOTE :**
1. Starting with Idle State
 2. Enter SR
 3. Change Frequency
 4. Clock must be stable tCKSRX
 5. Exit SR
 6. Set DLL on by MR1 A0=0
 7. Update Mode registers
 8. Any valid command

Figure 12. DLL Switch Sequence from DLL-off to DLL-on

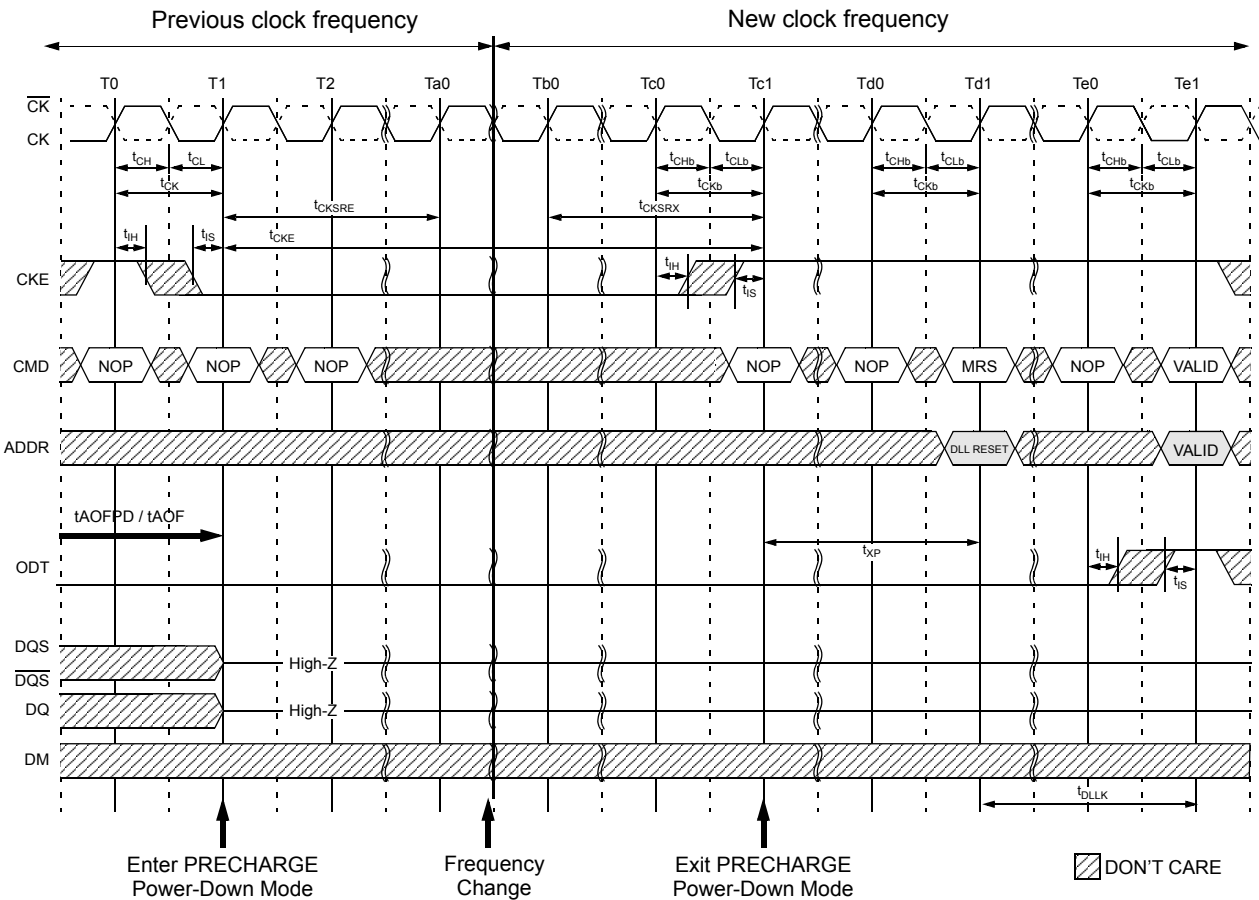
2.7 Input clock frequency change

Once the DDR3 SDRAM is initialized, the DDR3 SDRAM requires the clock to be "stable" during almost all states of normal operation. This means once the clock frequency has been set and is to be in the "stable state", the clock period is not allowed to deviate except for what is allowed for by the clock jitter and SSC (spread spectrum clocking) specifications.

The input clock frequency can be changed from one stable clock rate to another stable clock rate under two conditions:
 (1) Self-Refresh mode and (2) Precharge Power-down mode. Outside of these two modes, it is illegal to change the clock frequency.

For the first condition, once the DDR3 SDRAM has been successfully placed in to Self-Refresh mode and tCKSRE has been satisfied, the state of the clock becomes a don't care. Once a don't care, changing the clock frequency is permissible, provided the new clock frequency is stable prior to tCKSRX. When entering and exiting Self-Refresh mode for the sole purpose of changing the clock frequency, the Self-Refresh entry and exit specifications must still be met as outlined in See Figure 2.16. The DDR3 SDRAM input clock frequency is allowed to change only within the minimum and maximum operating frequency specified for the particular speed grade. Any frequency change below the minimum operating frequency would require the use of DLL_on-mode -> DLL_off -mode transition sequence, refer to "DLL on/off switching procedure" on page 19

The second condition is when the DDR3 SDRAM is in Precharge Power-down mode (either fast exit mode or slow exit mode). If the RTT_NOM feature was enabled in the mode register prior to entering Precharge power down mode, the ODT signal must continuously be registered LOW ensuring RTT is in an off state. If the RTT_NOM feature was disabled in the mode register prior to entering Precharge power down mode, RTT will remain in the off state. The ODT signal can be registered either LOW or HIGH in this case.. A minimum of tCKSRE must occur after CKE goes LOW before the clock frequency may change. The DDR3 SDRAM input clock frequency is allowed to change only within the minimum and maximum operating frequency specified for the particular speed grade. During the input clock frequency change, ODT and CKE must be held at stable LOW levels. Once the input clock frequency is changed, stable new clocks must be provided to the DRAM tCKSRX before Precharge Power-down may be exited; after Precharge Power-down is exited and tXP has expired, the DLL must be RESET via MRS. Depending on the new clock frequency additional MRS commands may need to be issued to appropriately set the WR, CL, and CWL with CKE continuously registered high. During DLL re-lock period, ODT must remain LOW and CKE must remain HIGH. After the DLL lock time, the DRAM is ready to operate with new clock frequency. This process is depicted in Figure 13 below.



- NOTE :**
1. Applicable for both SLOW EXIT and FAST EXIT Precharge Power-down
 2. tAOPFD and tAOF must be satisfied and outputs High-Z prior to T1; refer to ODT timing section for exact requirements
 3. If the RTT_NOM feature was enabled in the mode register prior to entering Precharge power down mode, the ODT signal must continuously be registered LOW ensuring RTT is in an off state, as shown in Figure 13. If the RTT_NOM feature was disabled in the mode register prior to entering Precharge power down mode, RTT will remain in the off state. The ODT signal can be registered either LOW or HIGH in this case.

Figure 13. Change Frequency during Precharge Power-down

2.8 Write Leveling

For better signal integrity, DDR3 memory module adopted fly by topology for the commands, addresses, control signals and clocks. The fly by topology has benefits from reducing number of stubs and their length but in other aspect, causes flight time skew between clock and strobe at every DRAM on DIMM. It makes it difficult for the Controller to maintain tDQSS, tDSS and tDSH specification. Therefore, the controller should support 'write leveling' in DDR3 SDRAM to compensate the skew.

The memory controller can use the 'write leveling' feature and feedback from the DDR3 SDRAM to adjust the $\overline{DQS} - DQS$ to $\overline{CK} - CK$ relationship. The memory controller involved in the leveling must have adjustable delay setting on $\overline{DQS} - DQS$ to align the rising edge of $\overline{DQS} - DQS$ with that of the clock at the DRAM pin. DRAM asynchronously feeds back $\overline{CK} - CK$, sampled with the rising edge of $\overline{DQS} - DQS$, through the DQ bus. The controller repeatedly delays $\overline{DQS} - DQS$ until a transition from 0 to 1 is detected.

The $\overline{DQS} - DQS$ delay established through this exercise would ensure tDQSS specification. Besides tDQSS, tDSS and tDSH specification also needs to be fulfilled. One way to achieve this is to combine the actual tDQSS in the application with an appropriate duty cycle and jitter on the $\overline{DQS} - DQS$ signals. Depending on the actual tDQSS in the application, the actual values for tDQSL and tDQSH may have to be better than the absolute limits provided in the chapter "AC Timing Parameters" in order to satisfy tDSS and tDSH specification. A conceptual timing of this scheme is shown in Figure 14.

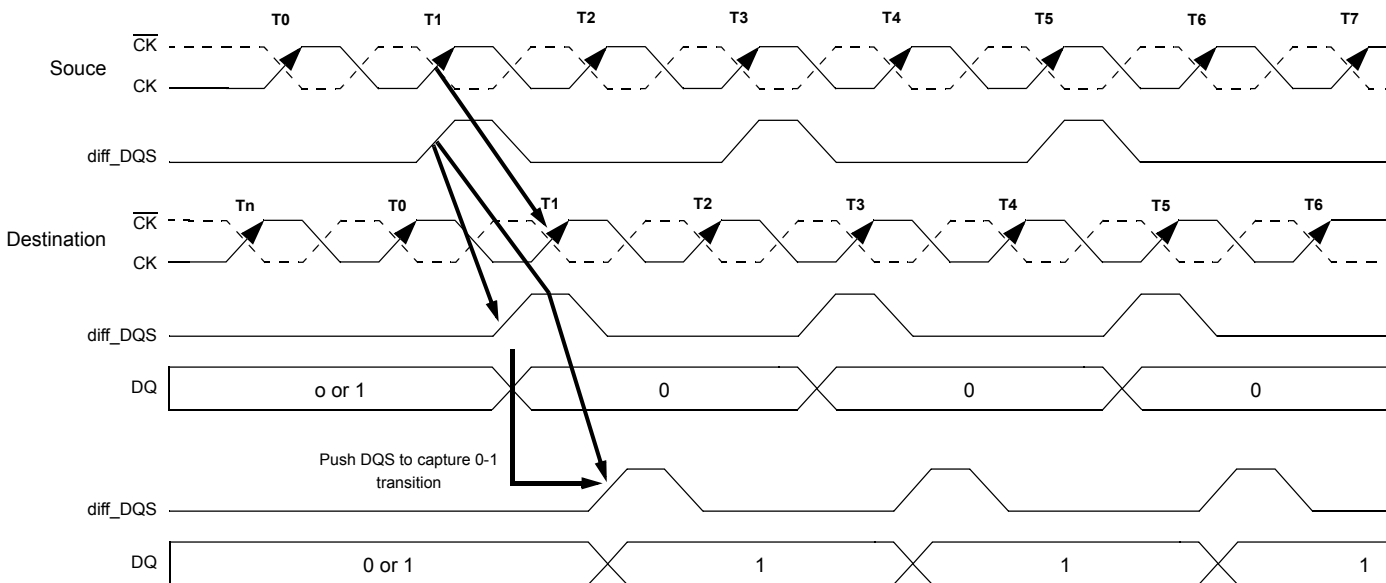


Figure 14. Write leveling concept

\overline{DQS}/DQS driven by the controller during leveling mode must be terminated by the DRAM based on ranks populated. Similarly, the DQ bus driven by the DRAM must also be terminated at the controller.

One or more data bits should carry the leveling feedback to the controller across the DRAM configurations X4, X8, and X16. On a X16 device, both byte lanes should be leveled independently. Therefore, a separate feedback mechanism should be available for each byte lane. The upper data bits should provide the feedback of the upper $\overline{diff_DQS}(\overline{diff_UDQS})$ to clock relationship whereas the lower data bits would indicate the lower $\overline{diff_DQS}(\overline{diff_LDQS})$ to clock relationship.

2.8.1 DRAM setting for write leveling & DRAM termination function in that mode

DRAM enters into Write leveling mode if A7 in MR1 set "High" and after finishing leveling, DRAM exits from write leveling mode if A7 in MR1 set "Low" (Table 7). Note that in write leveling mode, only \overline{DQS}/DQS terminations are activated and deactivated via ODT pin not like normal operation (Table 8).

[Table 7] MR setting involved in the leveling procedure

Function	MR1	Enable	Disable
Write leveling enable	A7	1	0
Output buffer mode (Qoff)	A12	0	1

[Table 8] DRAM termination function in the leveling mode

ODT pin @DRAM	\overline{DQS}/DQS termination	DQs termination
De-asserted	Off	Off
Asserted	On	Off

NOTE : In Write Leveling Mode with its output buffer disabled (MR1[bit7] = 1 with MR1[bit12] = 1) all RTT_Nom settings are allowed; in Write Leveling Mode with its output buffer enabled (MR1[bit7] = 1 with MR1[bit12] = 0) only RTT_Nom settings of RZQ/2, RZQ/4 and RZQ/6 are allowed.

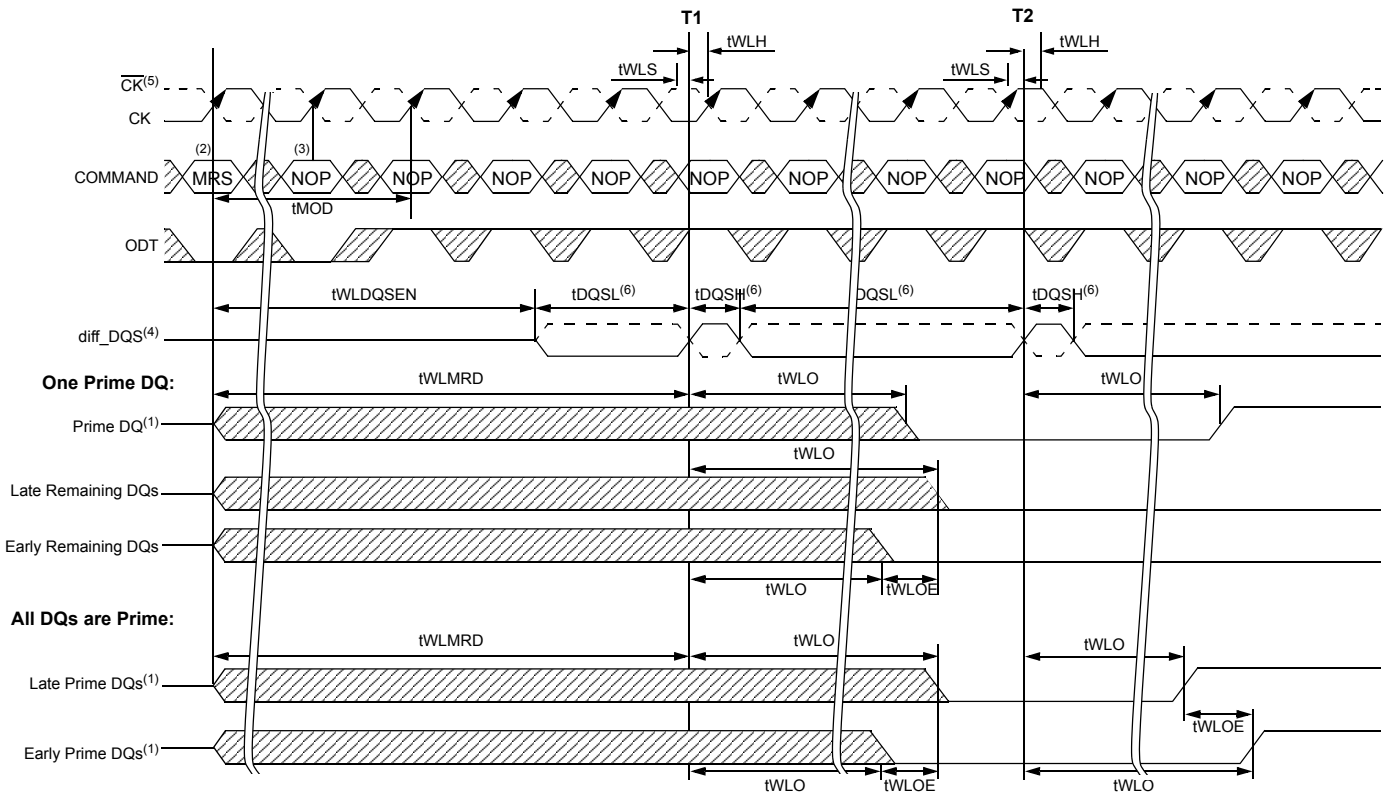
2.8.2 Procedure Description

The Memory controller initiates Leveling mode of all DRAMs by setting bit 7 of MR1 to 1. With entering write leveling mode, the DQ pins are in undefined driving mode. During write leveling mode, only NOP or DESELECT commands are allowed, as well as an MRS command to change Qoff bit (MR1[A12]) and an MRS command to exit (MR1[A7]). Upon exiting write leveling mode, the MRS command performing the exit (MR1[A7]=0) may also change MR1 bits of A12-A11, A9, A6-A5 and A2-A1. Since the controller levels one rank at a time, the output of other ranks must be disabled by setting MR1 bit A12 to 1. The controller may assert ODT after t_{MOD} , at which time the DRAM is ready to accept the ODT signal.

The Controller may drive DQS low and \overline{DQS} high after a delay of $t_{WLDQSEN}$, at which time DRAM has applied on-die termination on these signals. After t_{DQSL} and t_{WLMRD} , controller provides a single DQS, \overline{DQS} edge which is used by the DRAM to sample CK driven from controller. $t_{WLMRD}(max)$ timing is controller dependent.

DRAM samples CK status with rising edge of DQS and provides feedback on all the DQ bits asynchronously after t_{WLO} timing. There is a DQ output uncertainty of t_{WLOE} defined to allow mismatch on DQ bits; there are no read strobes (DQS/ \overline{DQS}) needed for these DQs. Controller samples incoming DQ and decides to increment or decrement DQS delay setting and launches the next DQS/ \overline{DQS} pulse after some time, which is controller dependent. Once a 0 to 1 transition is detected, the controller locks DQS delay setting and write leveling is achieved for the device.

Figure 15 describes the timing diagram and parameters for the overall Write Leveling procedure.



NOTE *:

1. DRAM has the option to drive leveling feedback on a prime DQ or all DQs. If feedback is driven only on one DQ, the remaining DQs must be driven low, as shown in above Figure, and maintained at this state through out the leveling procedure.
2. MRS : Load MR1 to enter write leveling mode
3. NOP : NOP or deselect
4. diff_DQS is the differential data strobe (DQS- \overline{DQS}). Timing reference points are the zero crossings. DQS is shown with solid line, \overline{DQS} is shown with dotted line
5. CK/ \overline{CK} : CK is shown with solid dark line, where as \overline{CK} is drawn with dotted line.
6. DQS, \overline{DQS} needs to fulfill minimum pulse width requirements $t_{DQSH}(min)$ and $t_{DQSL}(min)$ as defined for regular Writes; the max pulse width is system dependent

Figure 15. Timing details of Write leveling sequence [DQS- \overline{DQS} is capturing CK- \overline{CK} low at T1 and CK- \overline{CK} high at T2]

2.8.3 Write Leveling Mode Exit

The following sequence describes how the Write Leveling Mode should be exited:

1. After the last rising strobe (see ~T111) edge, stop driving the strobe signals (see ~T128). Note: From now on, DQ pins are in undefined driving mode, and will remain undefined, until tMOD after the respective MR command (see T145).
2. Drive ODT pin low (tIS must be satisfied) and keep it low. (see T128).
3. After the RTT is switched off, disable Write Level Mode via MR command (see T132).
4. After tMOD is satisfied (T145), a any valid command may be registered. (MR commands may already be issued after tMRD (see T136).

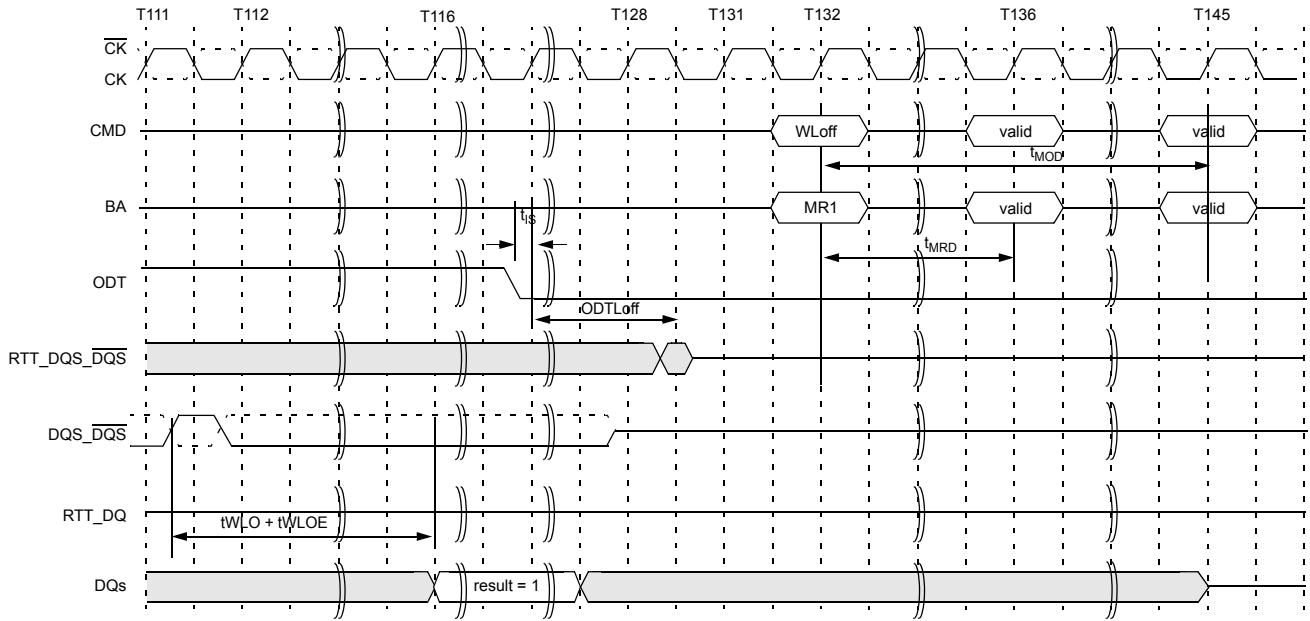


Figure 16. Timing details of Write leveling exit

2.9 Extended Temperature Usage

The following sequence describes how Write Leveling Mode should be exited:

1. After the last rising strobe (see ~T111) edge, stop driving the strobe signals (see ~T128). Note: From now on, DQ pins are in undefined driving mode, and will remain undefined, until tMOD after the respective MR command (T145).
2. Drive ODT pin low (tIS must be satisfied) and keep it low. (see T128).
3. After the RTT is switched off, disable Write Level Mode via MR command (see T132).
4. After tMOD is satisfied (T145), a any valid command may be registered. (MR commands may already be issued after tMRD (T136).

[Table 9] Mode Register Description

Field	Bits	Description
ASR	MR2(A6)	Auto Self-Refresh (ASR) (Optional) When enabled, DDR3 SDRAM automatically provides Self-Refresh power management functions for all supported operating temperature values. If not enabled, the SRT bit must be programmed to indicate T _{OPER} during subsequent Self-Refresh operation. 0 = Manual SR Reference (SRT) 1 = ASR enable (optional)
SRT	MR2(A7)	Self-Refresh Temperature (SRT) Range If ASR = 0, the SRT bit must be programmed to indicate T _{OPER} during subsequent Self-Refresh operation If ASR = 1, SRT bit must be set to 0b 0 = Normal operating temperature range 1 = Extended (optional) operating temperature range

2.9.1 Auto Self-Refresh mode - ASR Mode (optional)

DDR3 SDRAM provides an Auto Self-Refresh mode (ASR) for application ease. ASR mode is enabled by setting MR2 bit A6=1b and RR2 bit A7=0b. The DRAM will also manage Self-Refresh entry in either the Normal or Extended (optional) Temperature Ranges. In this mode, the DRAM will also manage Self-Refresh power consumption when the DRAM operating temperature changes, lower at low temperatures and higher at high temperatures.

If the ASR option is not supported by the DRAM, MR2 bit A6 must be set to 0b.

If the ASR mode is not enabled (MR2 bit. A6=0b), the SRT bit(MR2 A7) must be manually programmed with the operating temperature range required during Self-Refresh operation.

Support of the ASR option does not automatically imply support of the Extended Temperature Range and Auto Self-Refresh option availability.

2.9.2 Self-Refresh Temperature Range - SRT

SRT applies to devices supporting Extended Temperature Range only. If ASR = '0', the Self-Refresh Temperature (SRT) Range bit must be programmed to guarantee proper self-refresh operation. If SRT = '0', then the DRAM will set an appropriate refresh rate for Self-Refresh operation in the Normal Temperature Range. If SRT = '1' then the DRAM will set an appropriate, potentially different, refresh rate to allow Self-Refresh operation in either the Normal or Extended Temperature Ranges. The value of the SRT bit can effect self-refresh power consumption, please refer to the IDD table for details.

For parts that do not support the Extended Temperature Range, MR2 bit A7 must be set to '0' and the DRAM should not be operated outside the Normal Temperature Range.

Please refer to the component data sheet and/or the DIMM SPD for Extended Temperature Range availability.

[Table 10] Self-Refresh mode summary

MR2 A[6]	MR2 A[7]	Self-Refresh operation	Allowed Operating Temperature Range for Self-Refresh Mode
0	0	Self-refresh rate appropriate for the Normal Temperature Range	Normal (0 - 85 °C)
0	1	Self-refresh rate appropriate for either the Normal or Extended Temperature Ranges. The DRAM must support Extended Temperature Range. The value of the SRT bit can effect self-refresh power consumption, please refer to the IDD table for details.	Normal and Extended (0 - 95 °C)
1	0	ASR enabled (not supported). Self-Refresh power consumption is temperature dependent	Normal (0 - 85 °C)
1	0	ASR enabled (not supported). Self-Refresh power consumption is temperature dependent	Normal and Extended (0 - 95 °C)
1	1	Illegal	

2.10 Multi Purpose Register

The Multi Purpose Register (MPR) function is used to Read out a predefined system timing calibration bit sequence. The basic concept of the MPR is shown in Figure 17.

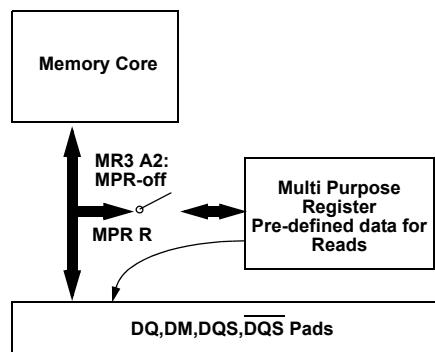


Figure 17. MPR Block Diagram

To enable the MPR, a MODE Register Set (MRS) command must be issued to MR3 Register with bit A2 = 1, as shown in Table 11. Prior to issuing the MRS command, all banks must be in the idle state (all banks precharged and tRP/tRPA met). Once the MPR is enabled, any subsequent RD or RDA commands will be redirected to the Multi Purpose Register. The resulting operation when a RD or RDA command is issued is defined by MR3 bits A[1:0] when the MPR is enabled as shown in Table 12. When the MPR is enabled, only RD or RDA commands are allowed until a subsequent MRS command is issued with the MPR disabled (MR3 bit A2 = 0). Power-Down mode, Self-Refresh, and any other non-RD/RDA command is not allowed during MPR enable mode. The RESET function is supported during MPR enable mode.

[Table 11] MPR MR3 Register Definition

MR3 A[2]	MR3 A[1:0]	Function
MPR	MPR-Loc	
0b	don't care (0b or 1b)	Normal operation, no MPR transaction. All subsequent Reads will come from DRAM array. All subsequent Write will go to DRAM array.
1b	see Table 14 on page 58	Enable MPR mode, subsequent RD/RDA commands defined by MR3 A[1:0].

2.10.1 MPR Functional Description

- One bit wide logical interface via all DQ pins during READ operation.
- Register Read on x4:
 - DQ[0] drives information from MPR.
 - DQ[3:0] drive the same information as DQ[0].
- Register Read on x8:
 - DQ[0] drives information from MPR.
 - DQ[7:1] drive the same information as DQ[0].
- Register Read on x16:
 - DQL[0] and DQU[0] drive information from MPR.
 - DQL[7:1] drive the same information as DQ[0].
- Addressing during for Multi Purpose Register reads for all MPR agents:
 - BA[2:0]: don't care
 - A[1:0]: A[1:0] must be equal to '00'. Data read burst order in nibble is fixed
 - A[2]: For BL=8, A[2] must be equal to 0b, burst order is fixed to [0,1,2,3,4,5,6,7], *) For Burst Chop 4 cases, the burst order is switched on nibble base A[2]=0b, Burst order: 0,1,2,3 *) A[2]=1b, Burst order : 4,5,6,7 *)
 - A[9:3]: don't care
 - A10/AP: don't care
 - A12/BC: Selects burst chop mode on-the-fly, if enabled within MR0.
 - A11, A13... (if available): don't care
- Regular interface functionality during register reads:
 - Support two Burst Ordering which are switched with A2 and A[1:0]=00.
 - Support of read burst chop (MRS and on-the-fly via A12/BC)
 - All other address bits (remaining column address bits including A10, all bank address bits) will be ignored by the DDR3 SDRAM.
 - Regular read latencies and AC timings apply.
 - DLL must be locked prior to MPR Reads.

NOTE* : Burst order bit 0 is assigned to LSB and burst order bit 7 is assigned to MSB of the selected MPR agent.

2.10.2 MPR Register Address Definition

Table 12 provides an overview of the available data locations, how they are addressed by MR3 A[1:0] during a MRS to MR3, and how their individual bits are mapped into the burst order bits during a Multi Purpose Register Read.

[Table 12] MPR MR3 Register Definition

MR3 A[2]	MR3 A[1:0]	Function	Burst Length	Read Address A[2:0]	Burst Order and Data Pattern
1b	00b	Read Predefined Pattern for System Calibration	BL8	000b	Burst order 0,1,2,3,4,5,6,7 Pre-defined Data Pattern [0,1,0,1,0,1,0,1]
			BC4	000b	Burst order 0,1,2,3 Pre-defined Data Pattern [0,1,0,1]
			BC4	100b	Burst order 4,5,6,7 Pre-defined Data Pattern [0,1,0,1]
1b	01b	RFU	BL8	000b	BL8 000b Burst order 0,1,2,3,4,5,6,7
			BC4	000b	BC4 000b Burst order 0,1,2,3
			BC4	100b	BC4 100b Burst order 4,5,6,7
1b	10b	RFU	BL8	000b	BL8 000b Burst order 0,1,2,3,4,5,6,7
			BC4	000b	BC4 000b Burst order 0,1,2,3
			BC4	100b	BC4 100b Burst order 4,5,6,7
1b	11b	RFU	BL8	000b	BL8 000b Burst order 0,1,2,3,4,5,6,7
			BC4	000b	BC4 000b Burst order 0,1,2,3
			BC4	100b	BC4 100b Burst order 4,5,6,7

NOTE : Burst order bit 0 is assigned to LSB and the burst order bit 7 is assigned to MSB of the selected MPR agent.

2.10.3 Relevant Timing Parameters

The following AC timing parameters are important for operating the Multi Purpose Register: tRP, tMRD, tMOD, and tMPRR. For more details refer to "Electrical Characteristics & AC Timing for DDR3-800 to DDR3-1600" on each component datasheet.

2.10.4 Protocol Example

Protocol Example (This is one example) : Read out predetermined read-calibration pattern.

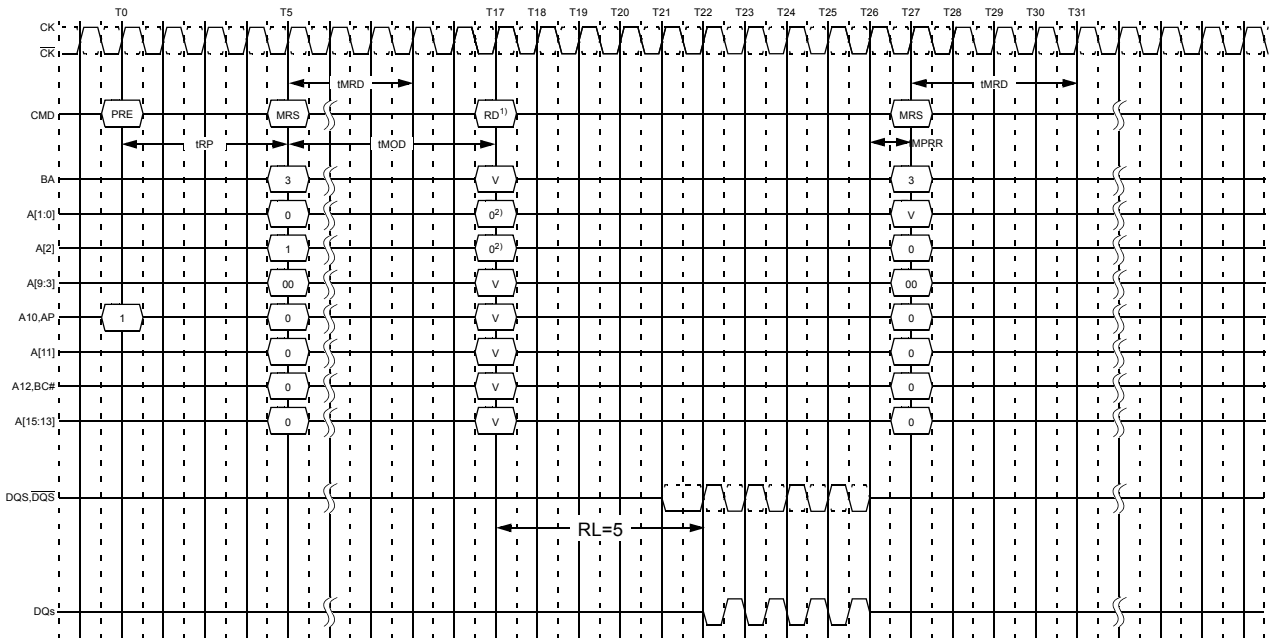
Description: Multiple reads from Multi Purpose Register, in order to do system level read timing calibration based on predetermined and standardized pattern.

Protocol Steps:

- Precharge All.
- Wait until tRP is satisfied.
- MRS MR3, Opcode "A2 = 1b" and "A[1:0] = 00b"
Redirect all subsequent reads into the Multi Purpose Register, and load Pre-defined pattern into MPR.
- Wait until tMRD and tMOD are satisfied (Multi Purpose Register is then ready to be read). During the period MR3 A2 =1, no data write operation is allowed.
- Read:
 - A[1:0] = '00'b (Data burst order is fixed starting at nibble, always '00b' here)
 - A[2] = '0'b (For BL=8, burst order is fixed as 0,1,2,3,4,5,6,7)
 - A12/BC = 1 (use regular burst length of 8)
 - All other address pins (including BA[2:0] and A10/AP): don't care

Readout of predefined pattern for system read calibration with BL8

(RL=5tCK, Fixed Burst order and Single Readout)



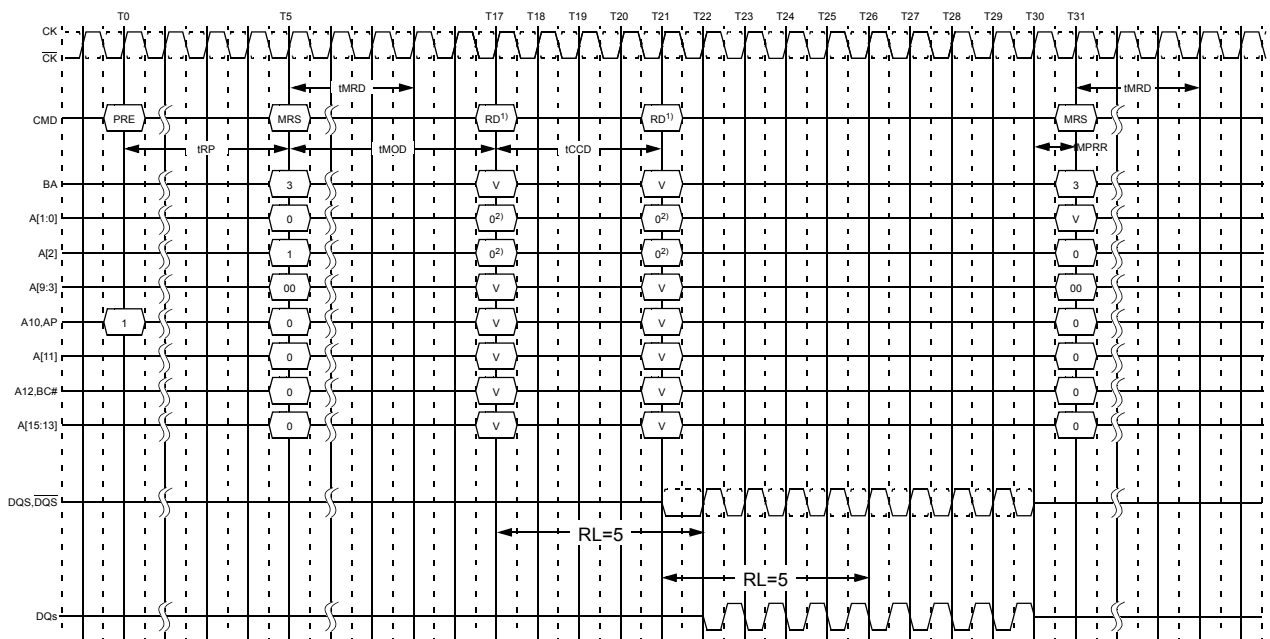
NOTE :

- 1) RD with BL8 either by MRS or On the fly
- 2) Memory Controller must drive Low on A[2:0]

Figure 18. MPR Readout of predefined pattern, BL8 fixed burst order, single readout

Readout of predefined pattern for system read calibration with BL8

(RL=5tCK, Fixed Burst order and Back-to-Back Readout)



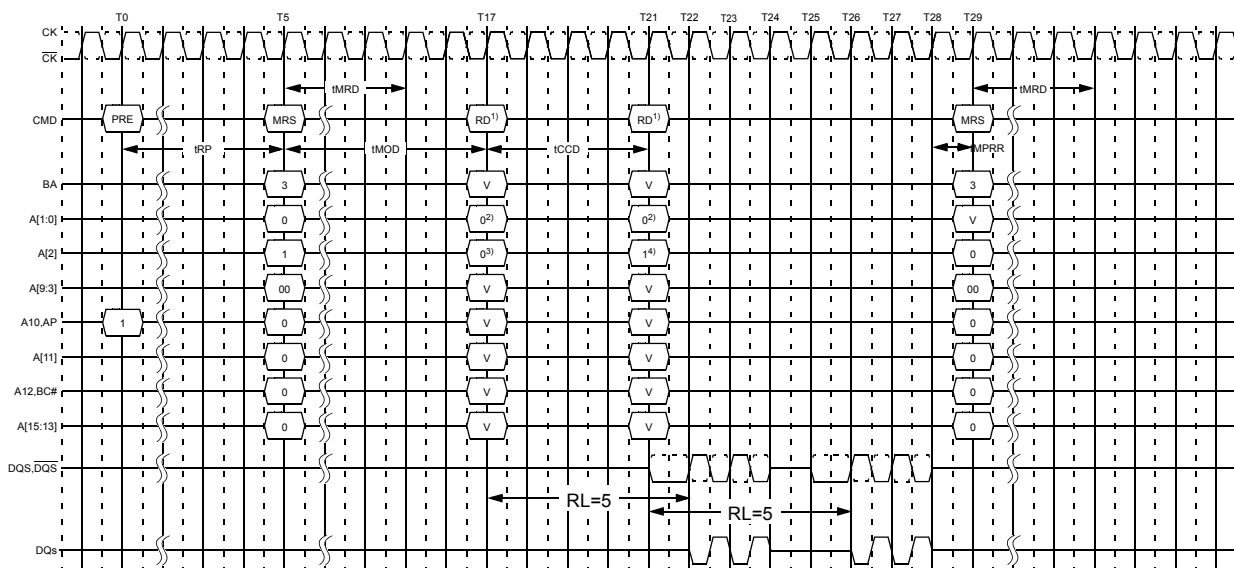
NOTE :

- 1) RD with BL8 either by MRS or On the fly
- 2) Memory Controller must drive Low on A[2:0]

Figure 19. MPR Readout of predefined pattern, BL8 fixed burst order, back-to-back readout

Readout of predefined pattern for system read calibration with BC4

(RL=5tCK, First Lower Nibble than Upper Nibble)



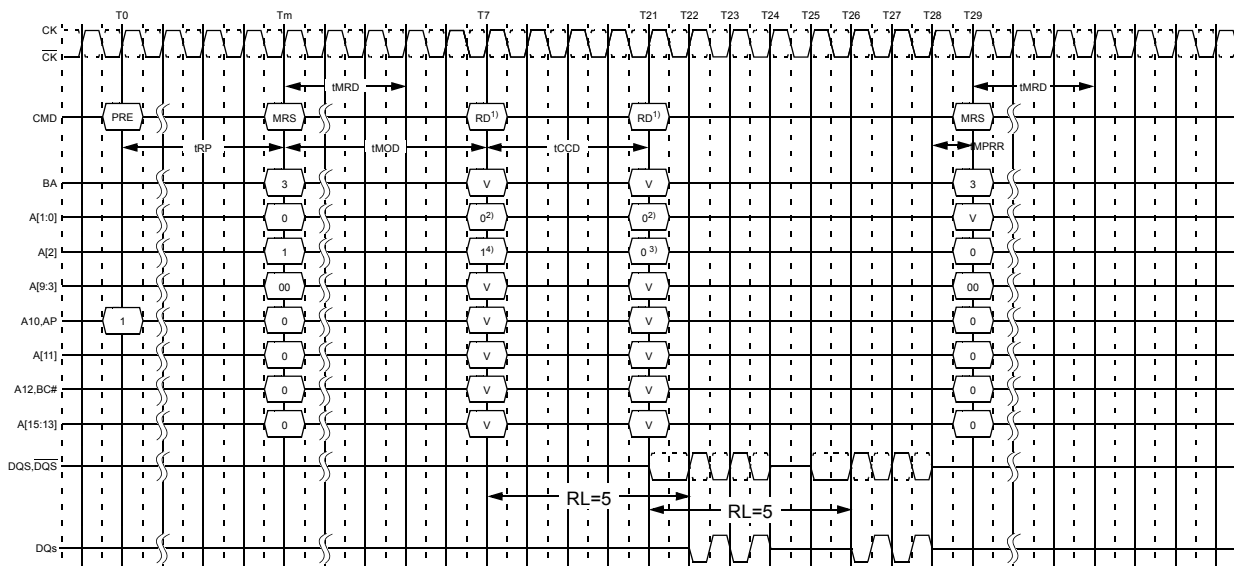
NOTE :

- 1) RD with BL4 either by MRS or On the fly
- 2) Memory Controller must drive Low on A[2:0]
- 3) A[2]=0 selects lower 4 nibble bits 0...3
- 4) A[2]=1 selects upper 4 nibble bits 4...7

Figure 20. MPR Readout predefined pattern, BC4, lower nibble then upper nibble

Readout of predefined pattern for system read calibration with BC4

(RL=5tCK, First Upper Nibble than Lower Nibble)



NOTE :

- 1) RD with BL4 either by MRS or On the fly
- 2) Memory Controller must drive Low on A[2:0]
- 3) A[2]=0 selects lower 4 nibble bits 0...3
- 4) A[2]=1 selects upper 4 nibble bits 4...7

Figure 21. MPR Readout of predefined pattern, BC4, upper nibble then lower nibble

2.11 ACTIVE Command

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0-BA2 inputs selects the bank, and the address provided on inputs A0-A15 selects the row. This row remains active (or open) for accesses until a precharge command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

2.12 PRECHARGE Command

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row activation a specified time (tRP) after the PRECHARGE command is issued, except in the case of concurrent auto precharge, where a READ or WRITE command to a different bank is allowed as long as it does not interrupt the data transfer in the current bank and does not violate any other timing parameters. Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command is allowed if there is no open row in that bank (idle state) or if the previously open row is already in the process of precharging. However, the precharge period will be determined by the last PRECHARGE command issued to the bank.

2.13 READ Operation

Any system or application incorporating random access memory products should be properly designed, tested and qualified to ensure proper use or access of such memory products. Disproportionate, excessive and/or repeated access to a particular address or addresses may result in reduction of product life.

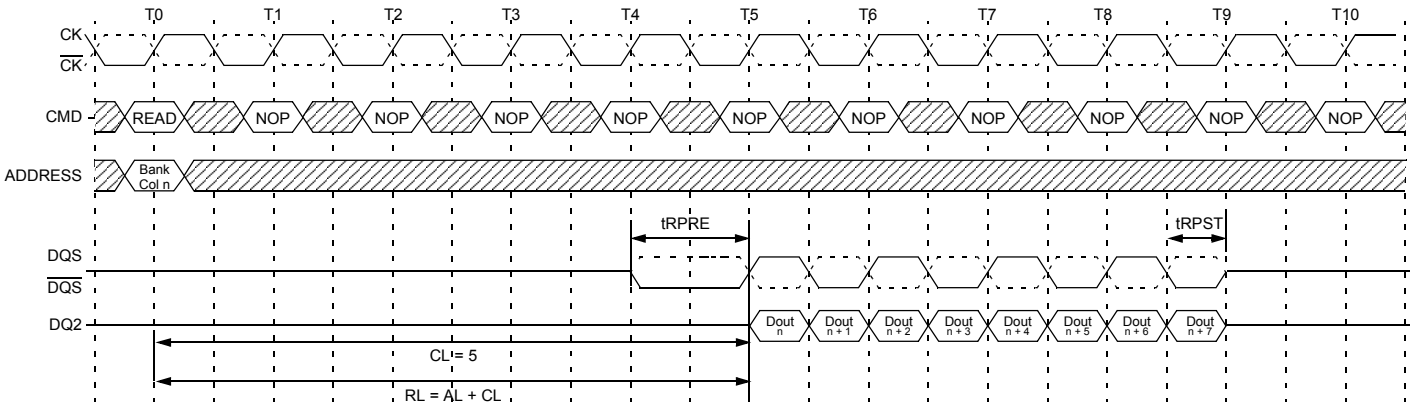
2.13.1 READ Burst Operation

During a READ or WRITE command, DDR3 will support BC4 and BL8 on the fly using address A12 during the READ or WRITE (AUTO PRECHARGE can be enabled or disabled).

A12 = 0, BC4 (BC4 = burst chop, tCCD = 4)

A12 = 1, BL8

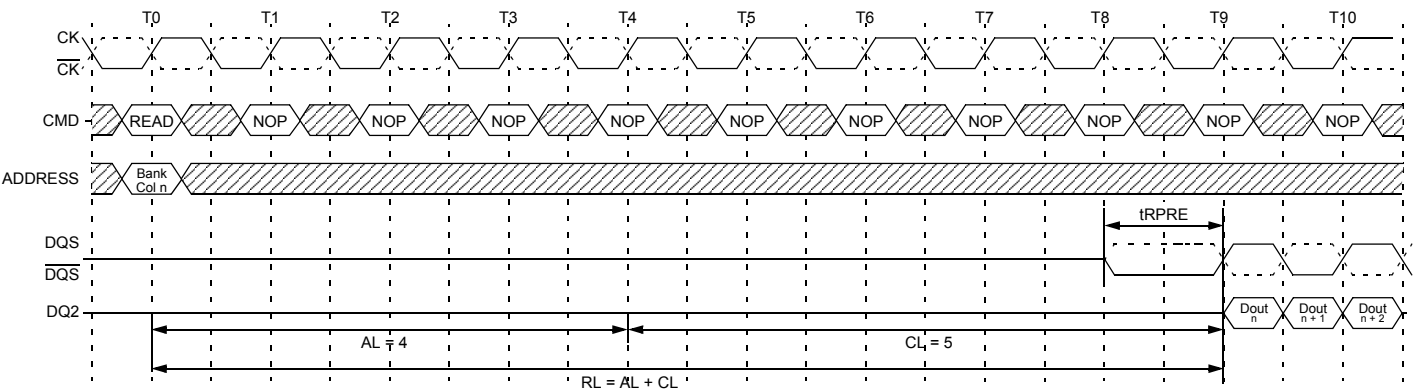
A12 is used only for burst length control, not as a column address.



NOTE :

1. BL8, RL = 5, AL = 0, CL = 5.
2. DOUT n = data-out from column n.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during READ command at T0.

Figure 22. READ Burst Operation RL = 5 (AL = 0, CL = 5, BL8)



NOTE :

1. BL8, RL = 9, AL = (CL - 1), CL = 5.
2. DOUT n = data-out from column n.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.

4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during READ command at T0.

Figure 23. READ Burst Operation RL = 9 (AL = 4, CL = 5, BL8)

2.13.2 READ Timing Definitions

Read timing is shown in Figure 24 and is applied when the DLL is enabled and locked.

Rising data strobe edge parameters:

- tDQSCK min/max describes the allowed range for a rising data strobe edge relative to CK, \overline{CK} .
- tDQSCK is the actual position of a rising strobe edge relative to CK, \overline{CK} .
- tQSH describes the DQS, \overline{DQS} differential output high time.
- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.

Falling data strobe edge parameters:

- tQSL describes the DQS, \overline{DQS} differential output low time.
- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.
- tDQSQ; both rising/falling edges of DQS, no tAC defined.

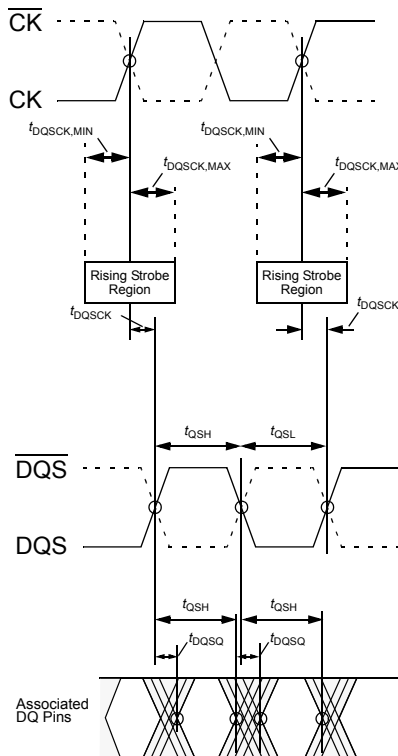


Figure 24. Read Timing Definition

2.13.2.1 DDR3 Clock to Data Strobe relationship

Clock to Data Strobe relationship is shown in Figure 25 and is applied when the DLL is enabled and locked.

Rising data strobe edge parameters:

- tDQSK min/max describes the allowed range for a rising data strobe edge relative to CK, \overline{CK} .
- tDQSK is the actual position of a rising strobe edge relative to CK, \overline{CK} .
- tQSH describes the data strobe high pulse width.

Falling data strobe edge parameters:

- tQSL describes the data strobe low pulse width.

tLZ(DQS), tHZ(DQS) for preamble/postamble (see 2.13.2.3 and Figure 27)

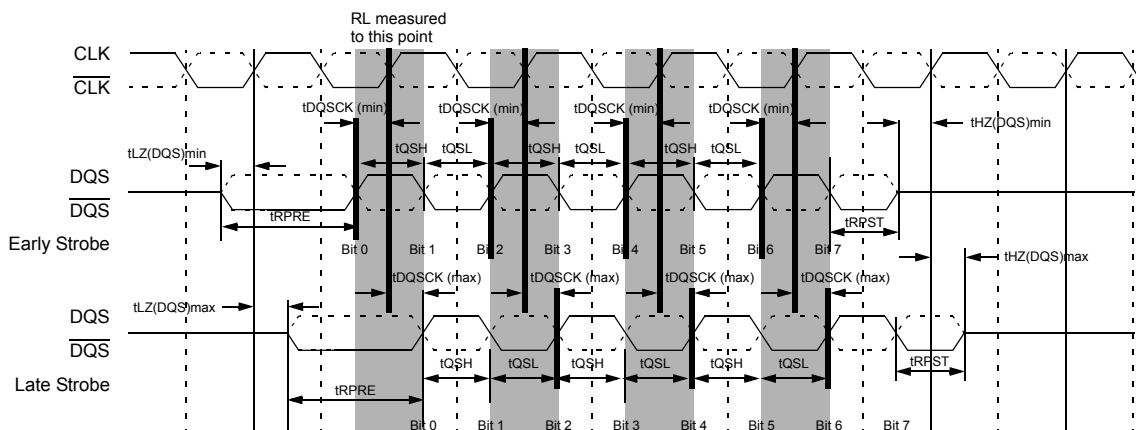


Figure 25. Clock to Data Strobe Relationship

NOTE :

1. Within a burst, rising strobe edge is not necessarily fixed to be always at tDQSK(min) or tDQSK(max). Instead, rising strobe edge can vary between tDQSK(min) and tDQSK(max).
2. Notwithstanding note 1, a rising strobe edge with tDQSK(max) at T(n) can not be immediately followed by a rising strobe edge with tDQSK(min) at T(n+1). This is because other timing relationships (tQSH, tQSL) exist:
if $tDQSK(n+1) < 0$:
$$tDQSK(n) < 1.0 tCK - (tQSHmin + tQSLmin) - |tDQSK(n+1)|$$
3. The DQS, \overline{DQS} differential output high time is defined by tQSH and the DQS, \overline{DQS} differential output low time is defined by tQSL.
4. Likewise, tLZ(DQS)min and tHZ(DQS)min are not tied to tDQSKmin (early strobe case) and tLZ(DQS)max and tHZ(DQS)max are not tied to tDQSKmax (late strobe case).
5. The minimum pulse width of read preamble is defined by tRPRE(min).
6. The maximum read postamble is bound by tDQSK(min) plus tQSH(min) on the left side and tHZ(DQS)max on the right side.
7. The minimum pulse width of read postamble is defined by tRPST(min).
8. The maximum read preamble is bound by tLZ(DQS)min on the left side and tDQSK(max) on the right side.

2.13.2.2 DDR3 Data Strobe to Data relationship

The Data Strobe to Data relationship is shown in Figure 26 and is applied when the DLL is enabled and locked.

Rising data strobe edge parameters:

- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.

Falling data strobe edge parameters:

- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.

tDQSQ; both rising/falling edges of DQS, no tAC defined

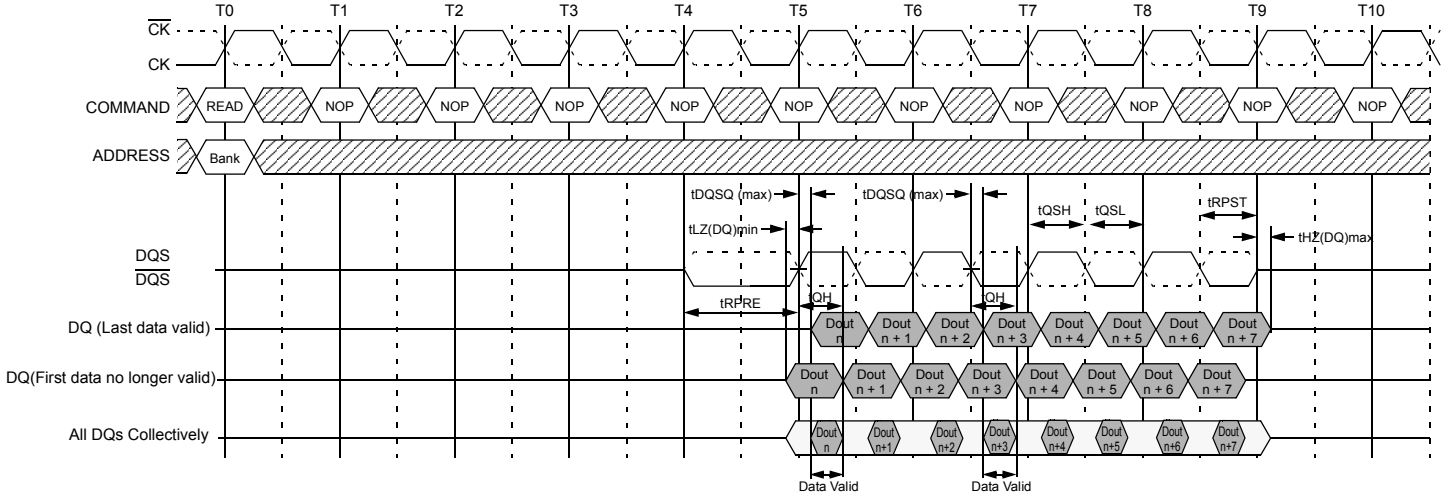


Figure 26. Data Strobe to Data Relationship

NOTE :

1. BL = 8, RL = 5 (AL = 0, CL = 5)
2. DOUT n = data-out from column n.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during READ command at T0.
5. Output timings are referenced to $V_{DDQ}/2$, and DLL on for locking.
6. tDQSQ defines the skew between DQS, DQS-bar to Data and does not define DQS, DQS-bar to Clock.
7. Early Data transitions may not always happen at the same DQ. Data transitions of a DQ can vary (either early or late) within a burst.

2.13.2.3 tLZ(DQS), tLZ(DQ), tHZ(DQS), tHZ(DQ) Calculation

tHZ and tLZ transitions occur in the same access time as valid data transitions. These parameters are referenced to a specific voltage level which specifies when the device output is no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS), tLZ(DQ). Figure 27 shows a method to calculate the point when device is no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS), tLZ(DQ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent. The parameters tLZ(DQS), tLZ(DQ), tHZ(DQS), and tHZ(DQ) are defined as singled ended.

tLZ(DQS): CK - CK-bar rising crossing at RL - 1
 tLZ(DQ): CK - CK-bar rising crossing at RL

tHZ(DQS), tHZ(DQ) with BL8: CK - CK-bar rising crossing at RL + 4 nCK
 tHZ(DQS), tHZ(DQ) with BC4: CK - CK-bar rising crossing at RL + 2 nCK

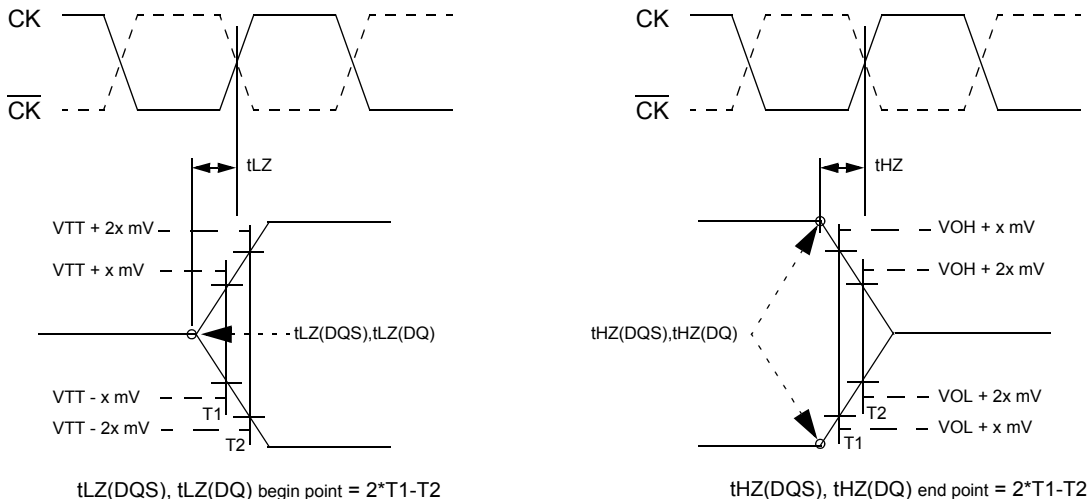


Figure 27. tLZ and tHZ method for calculating transitions and endpoints

2.13.2.4 tRPRE Calculation

Method for calculating differential pulse widths for tRPRE.

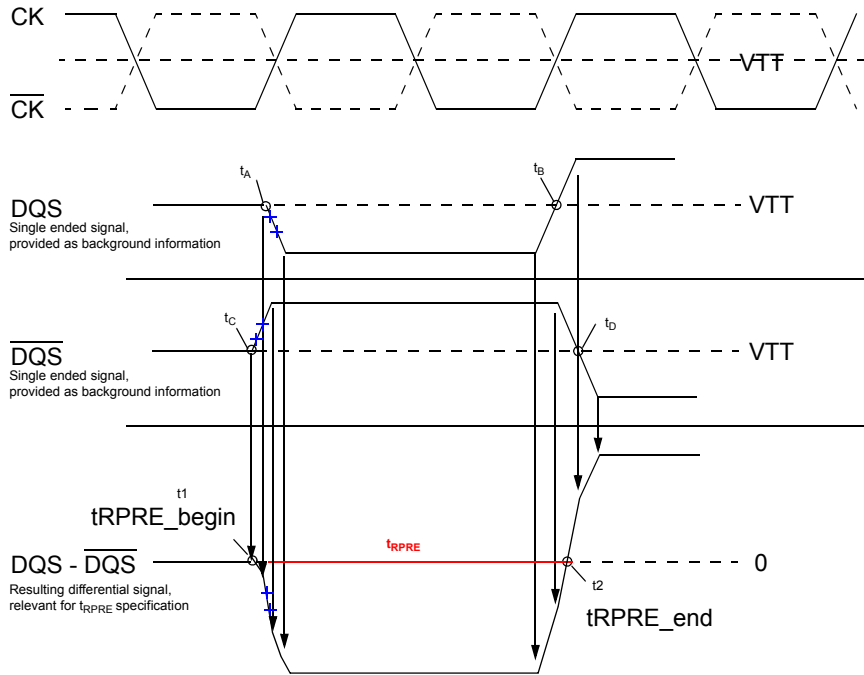


Figure 28. Method for calculating tRPRE transitions and endpoints

2.13.2.5 tRPST Calculation

Method for calculating differential pulse widths for tRPST.

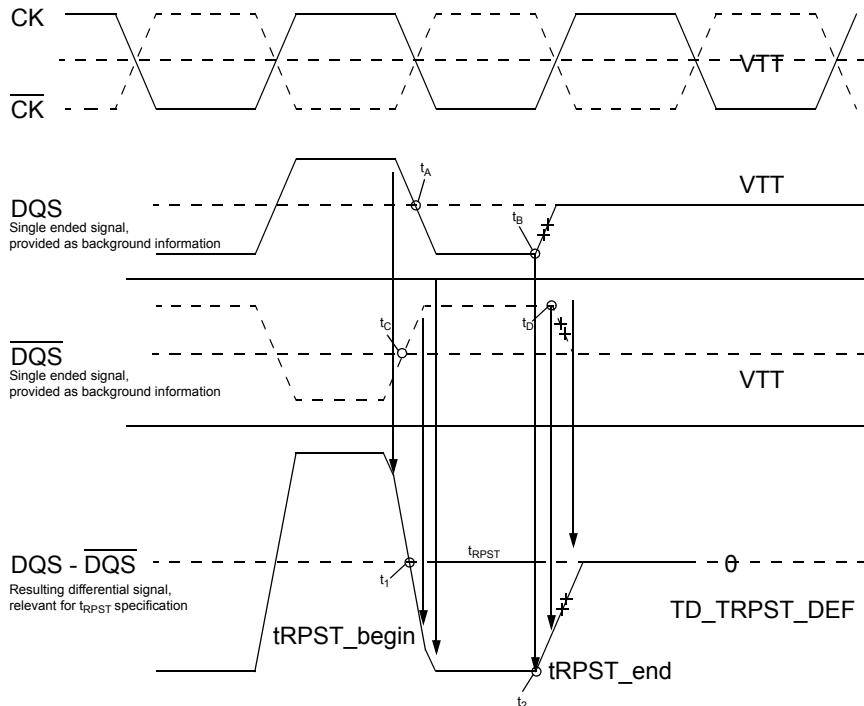
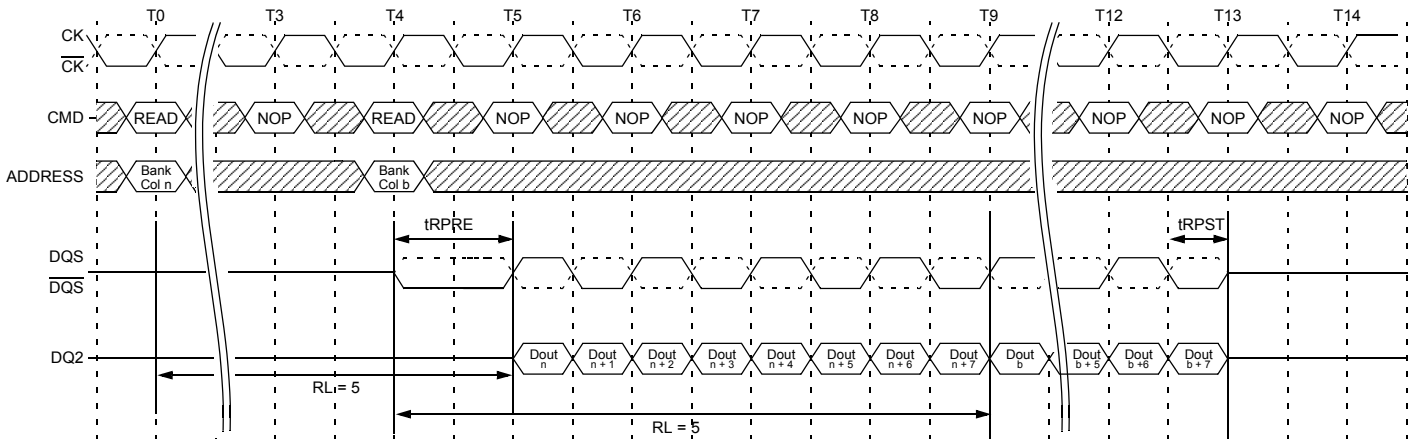


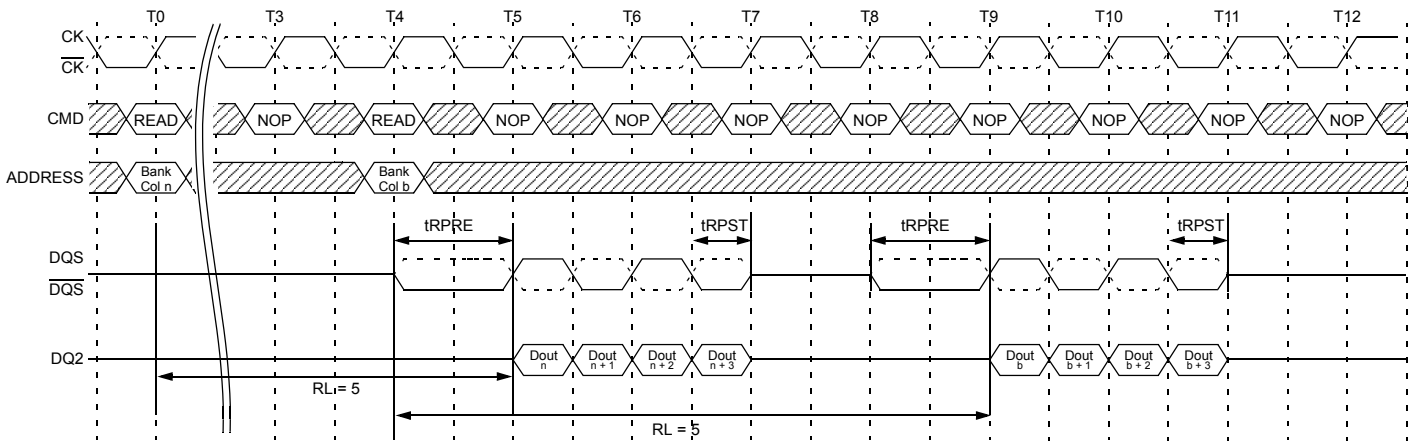
Figure 29. Method for calculating tRPST transitions and endpoints



NOTE :

1. BL8, RL = 5 (CL = 5, AL = 0)
2. Dout n (or b) = data-out from column n (or column b).
3. NOP commands are shown for ease of illustration ; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0=00] or MR0[A1:0 = 01]and A12 = 1 during READ commands at T0 and T4.

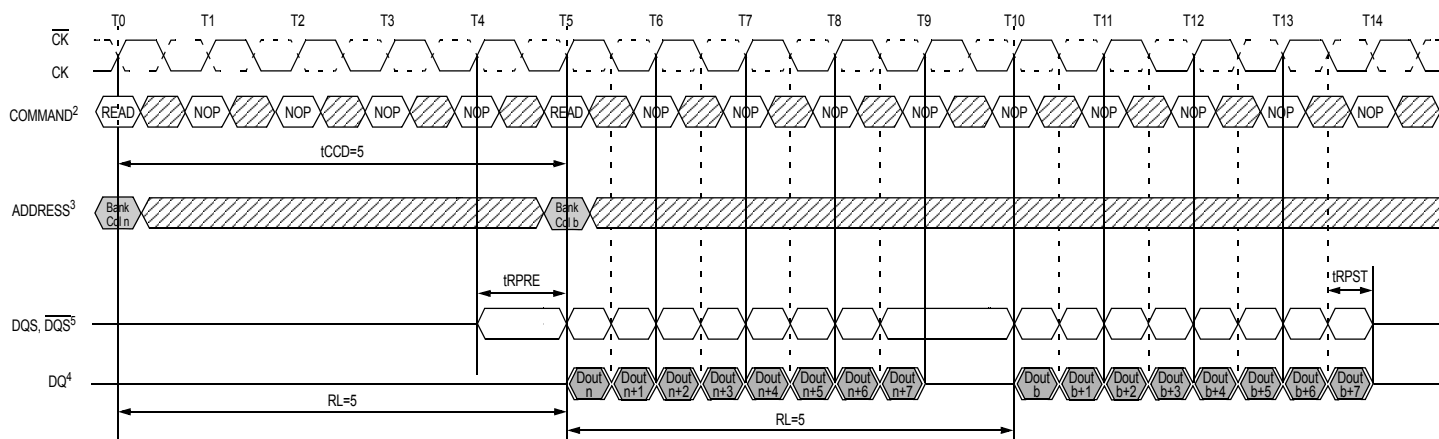
Figure 30. READ (BL8) to READ (BL8)



NOTE :

1. BL4, RL = 5 (CL = 5, AL = 0)
2. Dout n (or b) = data-out from column n (or column b).
3. NOP commands are shown for ease of illustration ; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0=00] or MR0[A1:0 = 01]and A12 = 0 during READ commands at T0 and T4.

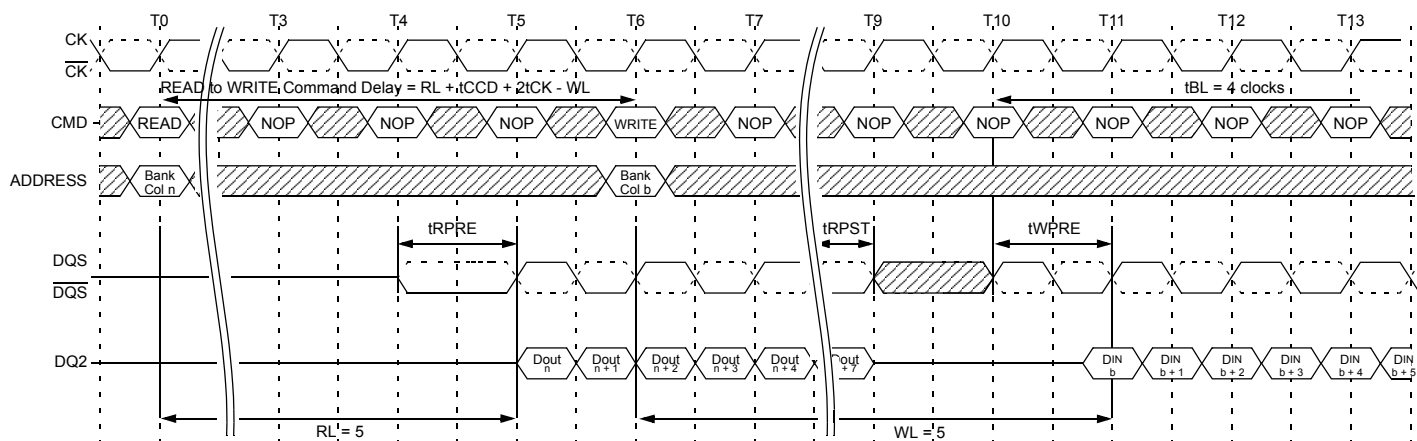
Figure 31. READ (BC4) to READ (BC4)



NOTE :

1. BL8, RL = 5 (CL = 5, AL = 0), tCCD=5
2. Dout n (or b) = data-out from column n (or column b).
3. NOP commands are shown for ease of illustration ; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0=00] or MR0[A1:0 = 01] and A12 = 1 during READ commands at T0 and T5.
5. DQS-DQS is held logic low at T9.

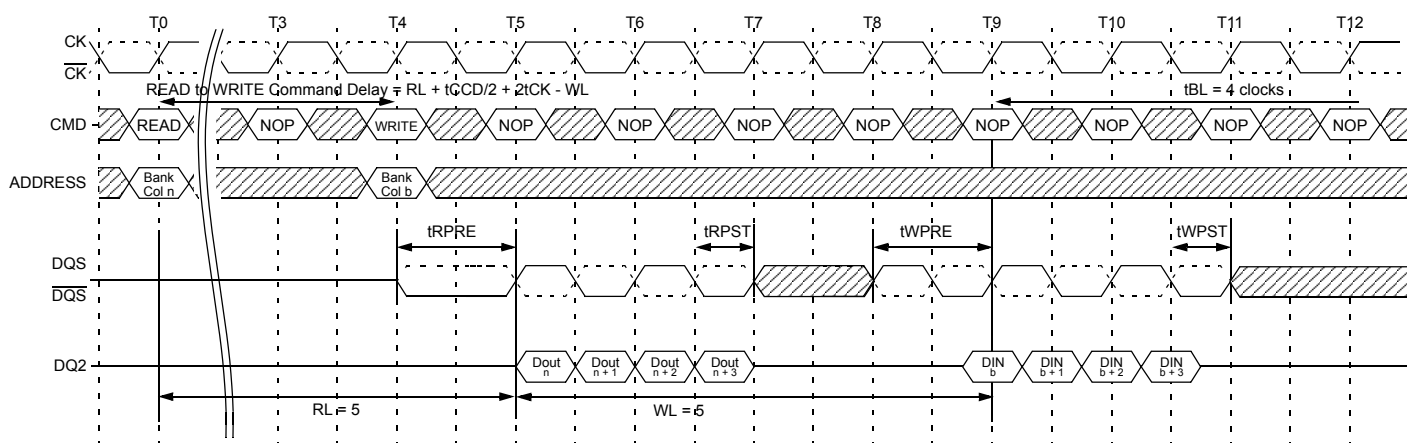
Figure 32. Nonconsecutive READ (BL8) to READ (BL8)



NOTE :

1. BL8, RL = 5 (CL = 5, AL = 0), WL = 5 (CWL = 5, AL = 0)
2. Dout n = data-out from column, DIN b = data-in from column b.
3. NOP commands are shown for ease of illustration ; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0=00] or MR0[A1:0 = 01] and A12 = 1 during READ commands at T0 and WRITE command at T6.

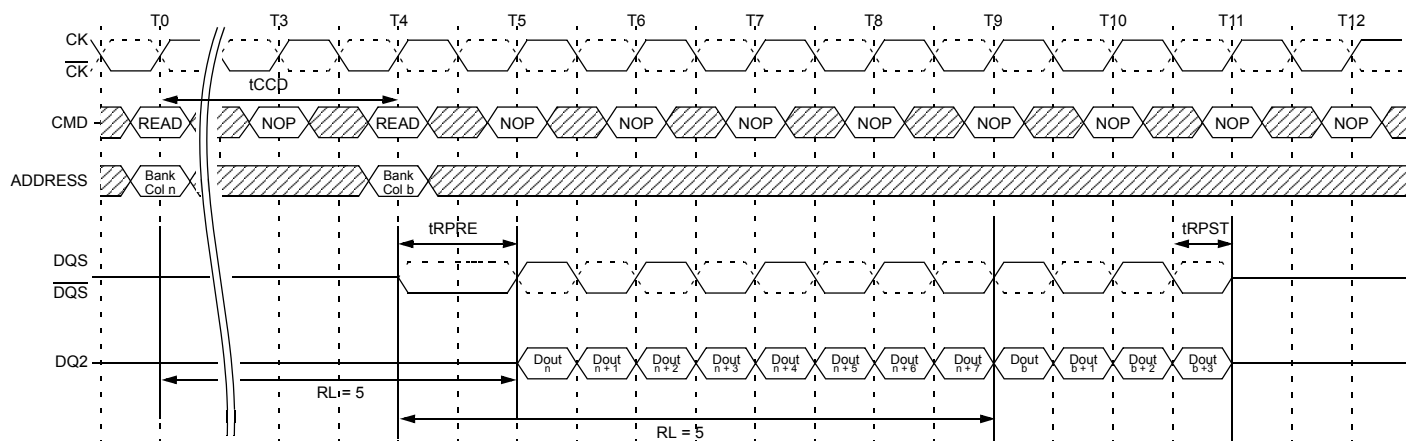
Figure 33. READ (BL8) to WRITE (BL8)



NOTE :

1. BL4, RL = 5 (CL = 5, AL = 0), WL = 5 (CWL = 5, AL = 0)
2. Dout n = data-out from column, DIN b = data-in from column b.
3. NOP commands are shown for ease of illustration ; other commands may be valid at these times.
4. BL4 setting activated by either MR0[A1:0=00] or MR0[A1:0 = 01] and A12 = 1 during READ commands at T0 and WRITE command at T4.

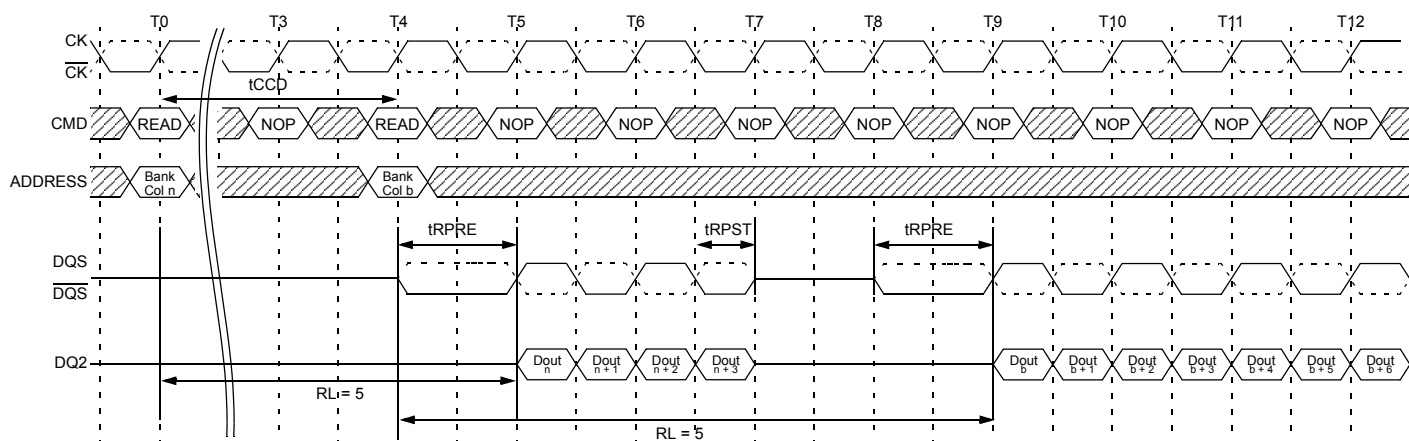
Figure 34. READ (BC4) to WRITE (BC4) OTF



NOTE :

1. RL = 5 (CL = 5, AL = 0)
2. Dout n (or b) = data-out from column n (or column b).
3. NOP commands are shown for ease of illustration ; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0=00] and A12 = 1 during READ commands at T0.
BC4 setting activated by either MR0[A1:0=01] and A12 = 0 during READ commands at T4.

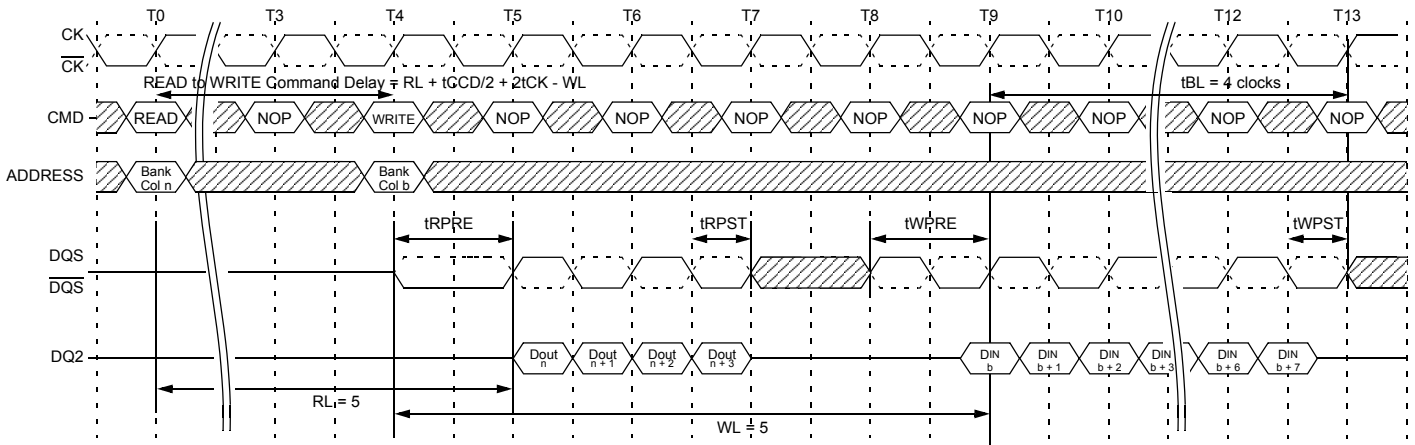
Figure 35. READ (BL8) to READ (BC4) OTF



NOTE :

1. RL = 5 (CL = 5, AL = 0)
2. Dout n (or b) = data-out from column n (or column b).
3. NOP commands are shown for ease of illustration ; other commands may be valid at these times.
4. BC4 setting activated by either MR0[A1:0=00] and A12 = 1 during READ commands at T0.
BL8 setting activated by either MR0[A1:0=01] and A12 = 0 during READ commands at T4.

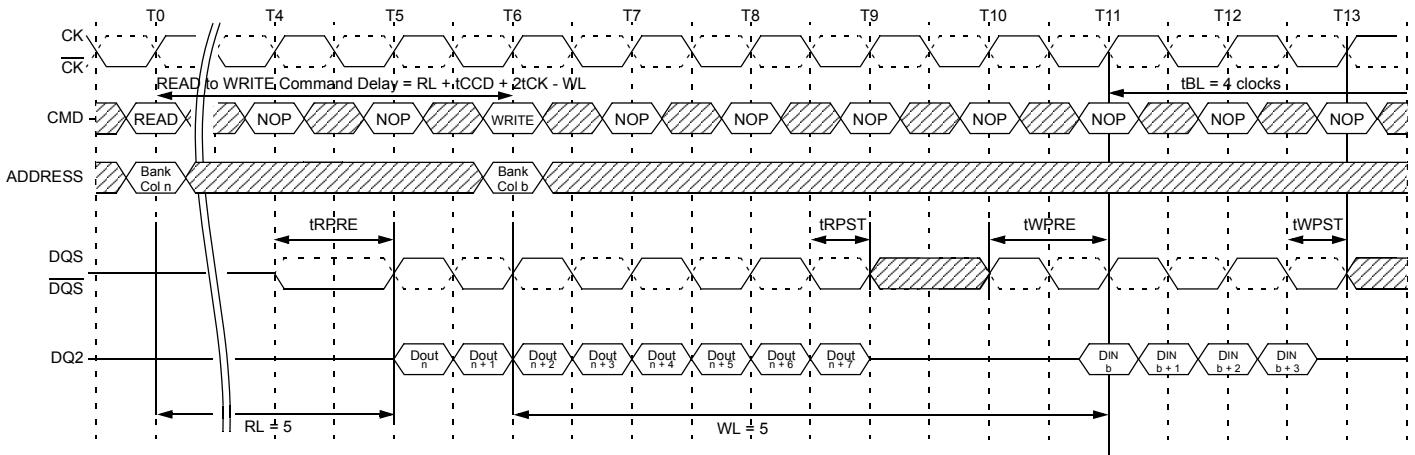
Figure 36. READ (BC4) to READ (BL8) OTF



NOTE :

1. RL = 5 (CL = 5, AL = 0), WL = 5 (CWL - 1, AL = 0)
2. Dout n = data-out from column, DIN b = data-in from column b.
3. NOP commands are shown for ease of illustration ; other commands may be valid at these times.
4. BC4 setting activated by either MR0[A1:0=00] and A12 = 0 during READ commands at T0.
BL8 setting activated by either MR0[A1:0=01] and A12 = 1 during WRITE commands at T4.

Figure 37. READ (BC4) to WRITE (BL8) OTF



NOTE :

1. RL = 5 (CL = 5, AL = 0), WL = 5 (CWL = 5, AL = 0)
2. Dout n = data-out from column, DIN b = data-in from column b.
3. NOP commands are shown for ease of illustration ; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0=00] and A12 = 1 during READ commands at T0.
BC4 setting activated by either MR0[A1:0=01] and A12 = 0 during WRITE commands at T6.

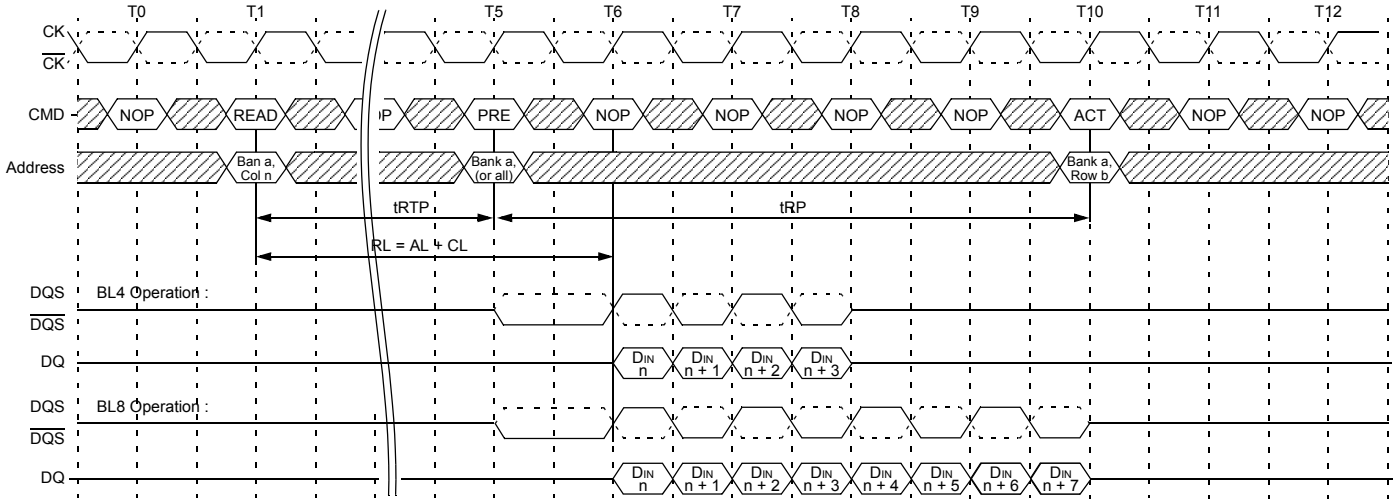
Figure 38. READ (BL8) to WRITE (BC4) OTF

2.13.3 Burst Read Operation followed by a Precharge

The minimum external Read command to Precharge command spacing to the same bank is equal to $AL + tRTP$ with $tRTP$ being the Internal Read Command to Precharge Command Delay. Note that the minimum ACT to PRE timing, $tRAS$, must be satisfied as well. The minimum value for the Internal Read Command to Precharge Command Delay is given by $tRTP.MIN = \max(4 \times nCK, 7.5 \text{ ns})$. A new bank active command may be issued to the same bank if the following two conditions are satisfied simultaneously:

1. The minimum RAS precharge time ($tRP.MIN$) has been satisfied from the clock at which the precharge begins.
2. The minimum RAS cycle time ($tRC.MIN$) from the previous bank activation has been satisfied.

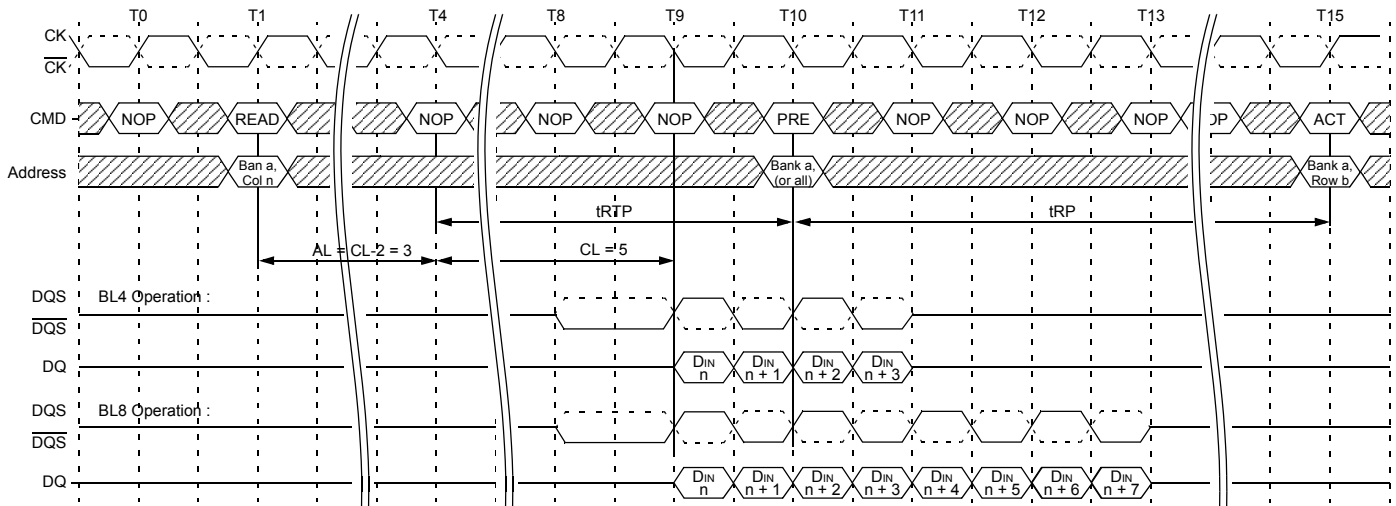
Examples of Read commands followed by Precharge are shown in Figure 39 and Figure 40.



NOTE :

1. $RL = 5$ ($CL = 5, AL = 0$)
2. $DOUT\ n =$ data-out from column n .
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. The example assumes $tRAS.MIN$ is satisfied at Precharge command time ($T5$) and that $tRC.MIN$ is satisfied at the next Active command time ($T10$).

Figure 39. READ to PRECHARGE, $RL=5, AL=0, CL=5, tRTP=4, tRP=5$



NOTE :

1. $RL = 8$ ($CL = 5, AL = CL - 2$)
2. $DOUT\ n =$ data-out from column n .
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. The example assumes $tRAS.MIN$ is satisfied at Precharge command time ($T10$) and that $tRC.MIN$ is satisfied at the next Active command time ($T15$).

Figure 40. READ to RRECHARGE, $RL=8, AL=CL-2, CL=5, tRTP=6, tRP=5$

2.14 WRITE Operation

2.14.1 DDR3 Burst Operation

During a READ or WRITE command, DDR3 will support BC4 and BL8 on the fly using address A12 during the READ or WRITE (AUTO PRECHARGE can be enabled or disabled).

A12 = 0, BC4 (BC4 = burst chop, tCCD = 4)

A12 = 1, BL8

A12 is used only for burst length control, not as a column address.

2.14.2 WRITE Timing Violations

2.14.2.1 Motivation

Generally, if timing parameters are violated, a complete reset/initialization procedure has to be initiated to make sure the DRAM works properly. However, it is desirable for certain minor violations that the DRAM is guaranteed not to "hang up" and errors be limited to that particular operation. (for reference: add more motivation here later, or refer to the "Read Synchronization" section if available) For the following, it will be assumed that there are no timing violations w.r.t. to the Write command itself (including ODT, etc.) and that it does satisfy all timing requirements not mentioned below.

2.14.2.2 Data Setup and Hold Violations

Should the data to strobe timing requirements (tDS, tDH) be violated, for any of the strobe edges associated with a write burst, then wrong data might be written to the memory location addressed with this WRITE command. In the example (Figure 41 on page 42), the relevant strobe edges for write burst A are associated with the clock edges: T5, T5.5, T6, T6.5, T7, T7.5, T8, T8.5. Subsequent reads from that location might result in unpredictable read data, however the DRAM will work properly otherwise.

2.14.2.3 Strobe to Strobe and Strobe to Clock Violations

Should the strobe timing requirements (tDQSH, tDQSL, tWPRE, tWPST) or the strobe to clock timing requirements (tDSS, tDSH, tDQSS) be violated, for any of the strobe edges associated with a Write burst, then wrong data might be written to the memory location addressed with the offending WRITE command. Subsequent reads from that location might result in unpredictable read data, however the DRAM will work properly otherwise.

In the example (Figure 41 on page 42) the relevant strobe edges for Write burst A are associated with the clock edges: T4, T4.5, T5, T5.5, T6, T6.5, T7, T7.5, T8, T8.5 and T9. Any timing requirements starting or ending on one of these strobe edges need to be fulfilled for a valid burst.

For Write burst B the relevant edges are T8, T8.5, T9, T9.5, T10, T10.5, T11, T11.5, T12, T12.5 and T13. Some edges are associated with both bursts.

2.14.2.4 Write Timing Parameters

This drawing is for example only to enumerate the strobe edges that "belong" to a Write burst. No actual timing violations are shown here. For a valid burst all timing parameters for each edge of a burst need to be satisfied (not only for one edge - as shown).

2.14.4 tWPRE Calculation

Method for calculating differential pulse widths for tWPRE is shown in Figure

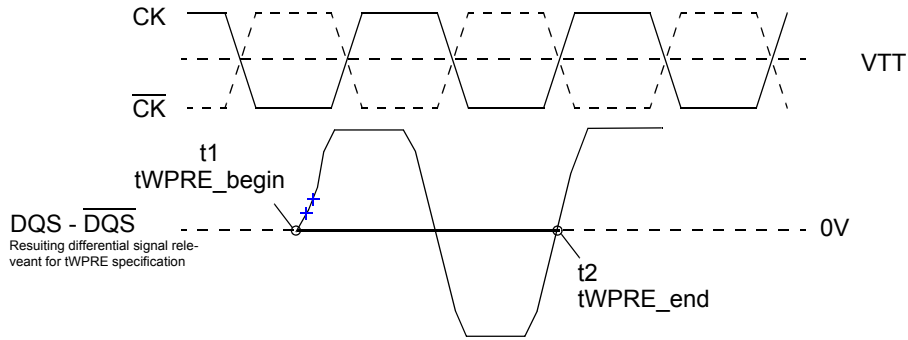


Figure 42. Method for calculating tWPRE transitions and endpoints

2.14.5 tWPST Calculation

Method for calculating differential pulse widths for tWPST is shown in Figure

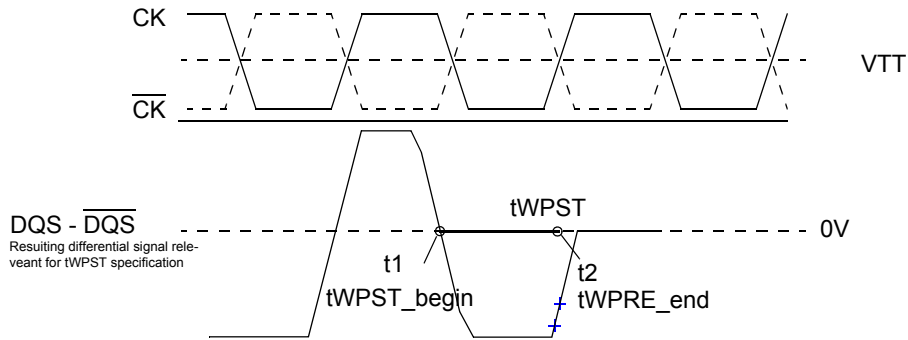
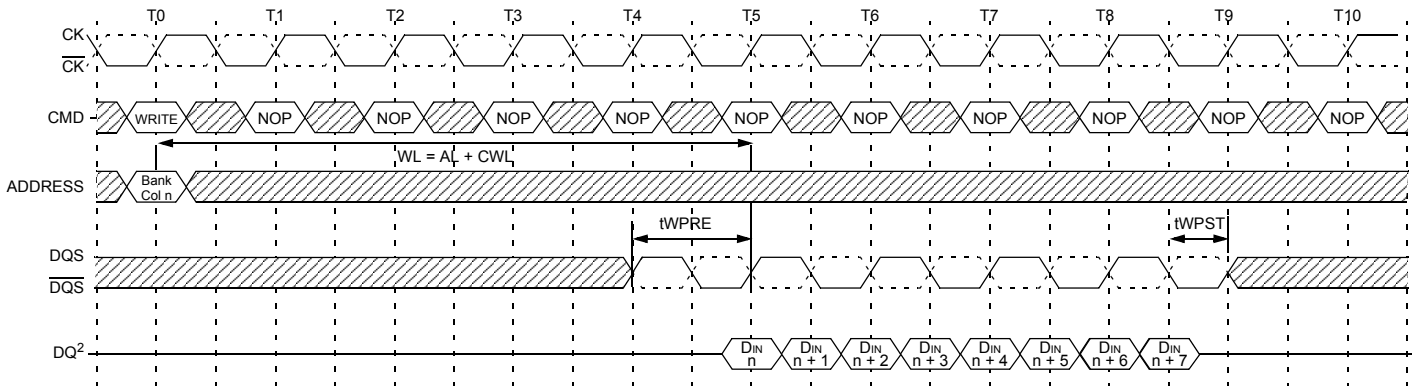
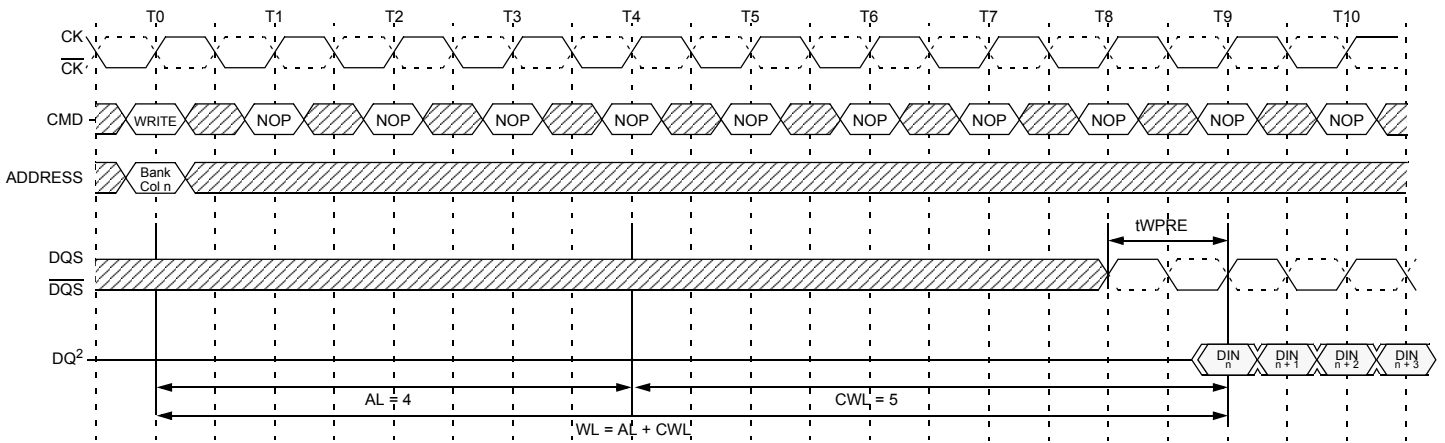


Figure 43. Method for calculating tWPST transitions and endpoints



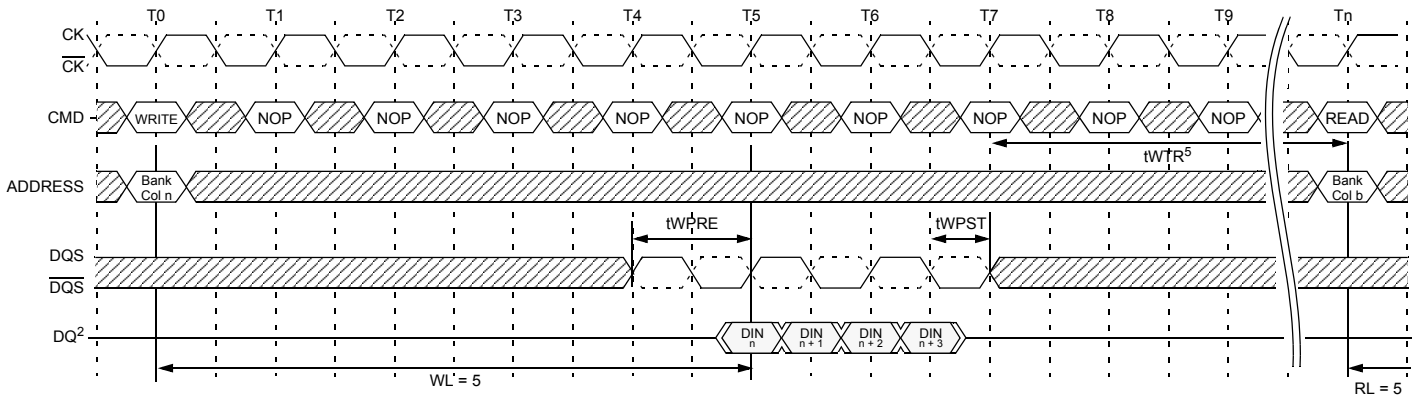
- NOTE :**
1. BL8, WL = 5, AL = 0, CWL = 5
 2. DIN n = data-in from column n.
 3. NOP commands are shown for ease of illustration ; other commands may be valid at these times.
 4. BL8 setting activated by either MR0[A1:0=00] or MR0[A1:0=01] and A12 = 1 during WRITE commands at T0.

Figure 44. WRITE Burst Operation WL=5 (AL=0, CWL=5, BL8)



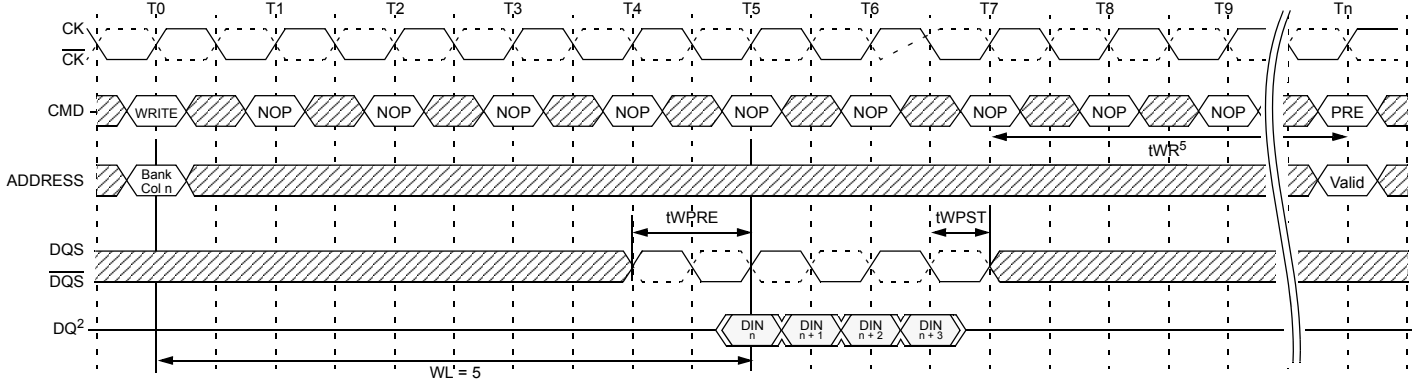
- NOTE :**
1. BL8, WL = 9, AL = (CL - 1), CL = 5, CWL = 5
 2. DIN n = data-in from column n.
 3. NOP commands are shown for ease of illustration ; other commands may be valid at these times.
 4. BL8 setting activated by either MR0[A1:0=00] or MR0[A1:0=01] and A12 = 1 during WRITE commands at T0.

Figure 45. WRITE Burst Operation WL=9 (AL=CL-1, CWL=5, BL8)



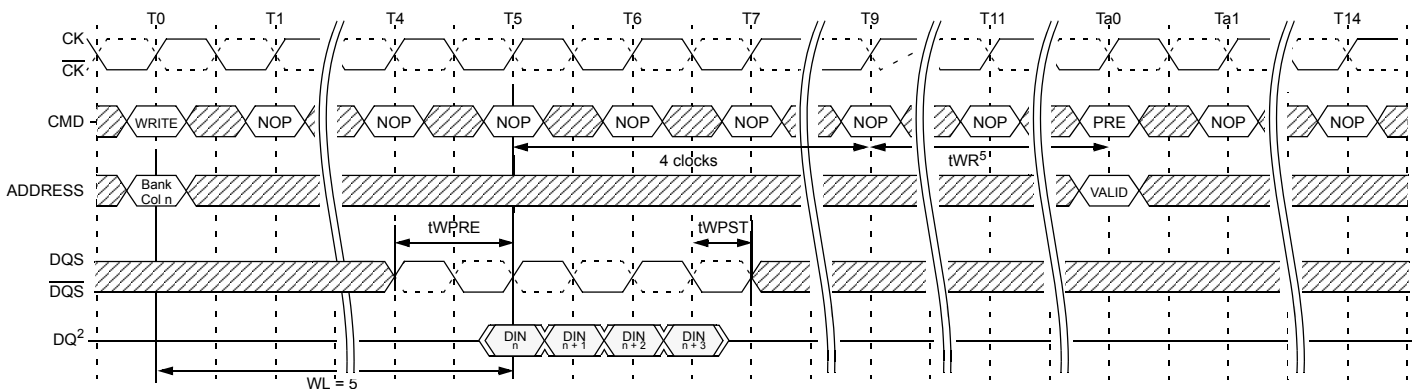
- NOTE :**
1. BC4, WL = 5, RL = 0
 2. DIN n = data-in from column n ; Dout b = data-out from column b.
 3. NOP commands are shown for ease of illustration ; other commands may be valid at these times.
 4. BC4 setting activated by MRO[A1:0=10] during WRITE commands at T0 and READ command at Tn.
 5. tWTR controls the write to read delay to the same device and starts with the first rising clock edge after the last write data shown at T7.

Figure 46. WRITE (BC4) to READ (BC4) Operation



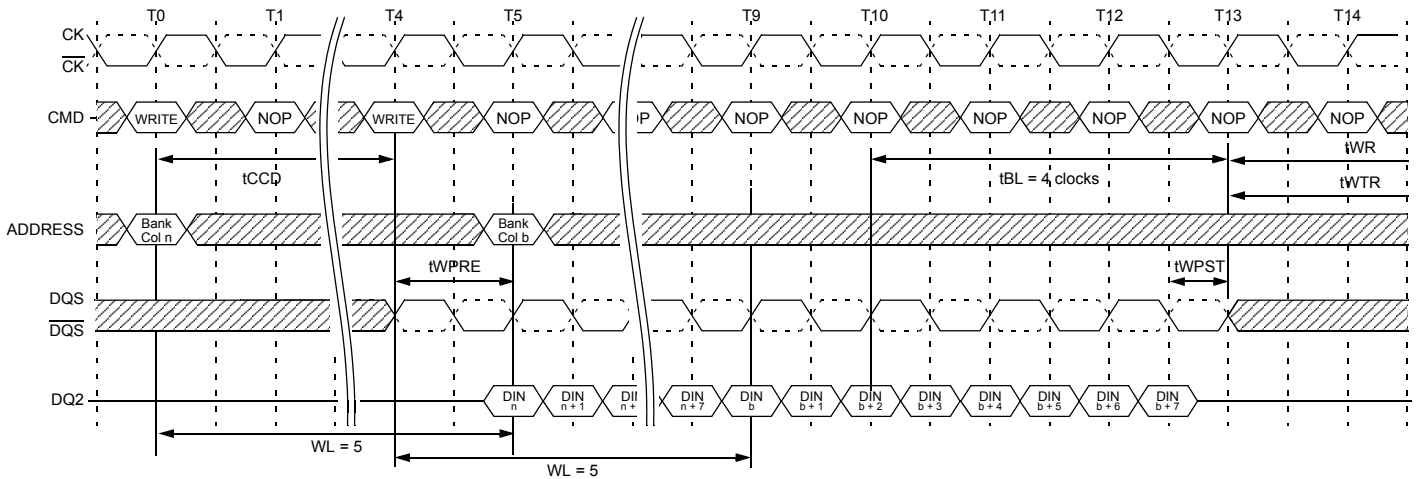
- NOTE :**
1. BC4, WL = 5, RL = 5.
 2. DIN n = data-in from column n ; DOOUT b = data-out from column b.
 3. NOP commands are shown for ease of illustration ; other commands may be valid at these times.
 4. BC4 setting activated by MRO[A1:0 = 10] during WRITE command at T0.
 5. The write recovery time (tWR) referenced from the first rising clock edge after the last write data shown at T7. tWR specifies the last burst write cycle until the precharge command can be issued to the same bank.

Figure 47. WRITE (BC4) to PRECHARGE Operation



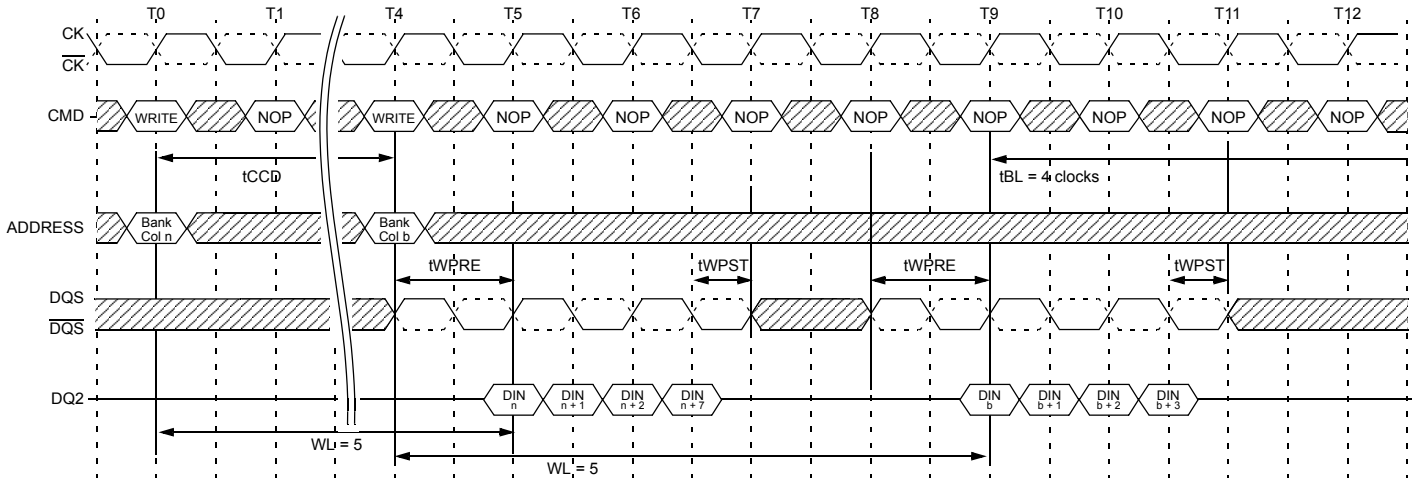
- NOTE :**
1. BC4 OTF, WL = 5 (CWL = 5, AL = 0)
 2. DIN n (or b) = data-in from column n.
 3. NOP commands are shown for ease of illustration ; other commands may be valid at these times.
 4. BC4 OTF setting activated by MRO[A1:0 = 01] and A12 = 0 during WRITE command at T0.
 5. The write recovery time (tWR) starts at the rising clock edge T9 (4 clocks from T5).

Figure 48. WRITE (BC4) OTF to PRECHARGE Operation



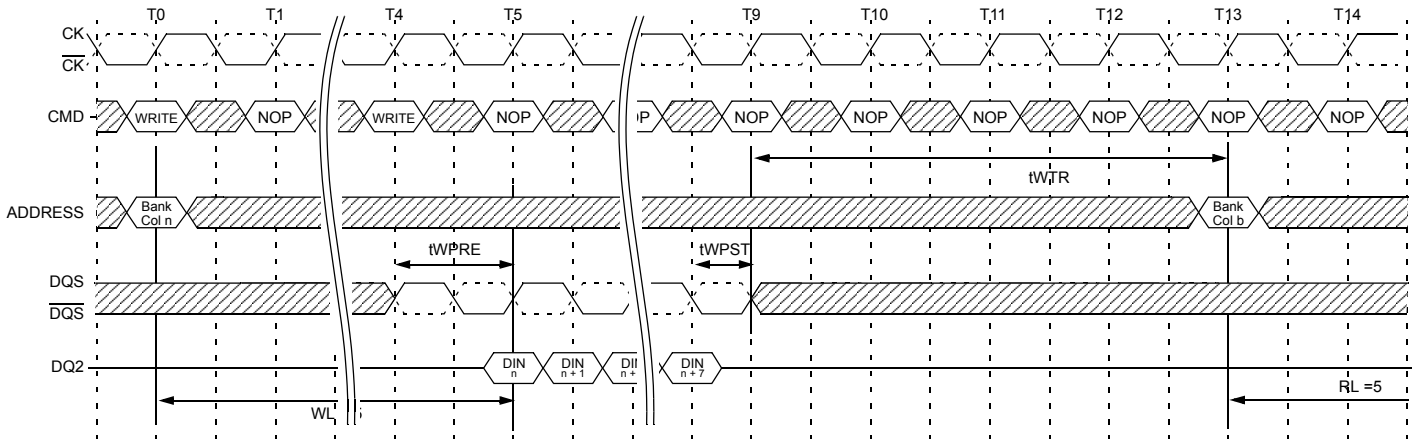
- NOTE :**
1. BL8, WL = 5(CWL = 5, AL = 0)
 2. DIN n (or b) = data-in from column n (or column b.)
 3. NOP commands are shown for ease of illustration ; other commands may be valid at these times.
 4. BL8 setting activated by either MR0[A1:0=00] or MR0[A1:0=01] and A12 = 1 during WRITE commands at T0 and T4
 5. The write recovery time(tWR) and write timing parmeter (tWTR) are referenced from the first rising clock edge after the last write data shown at T13.

Figure 49. WRITE (BL8) to WRITE (BL8)



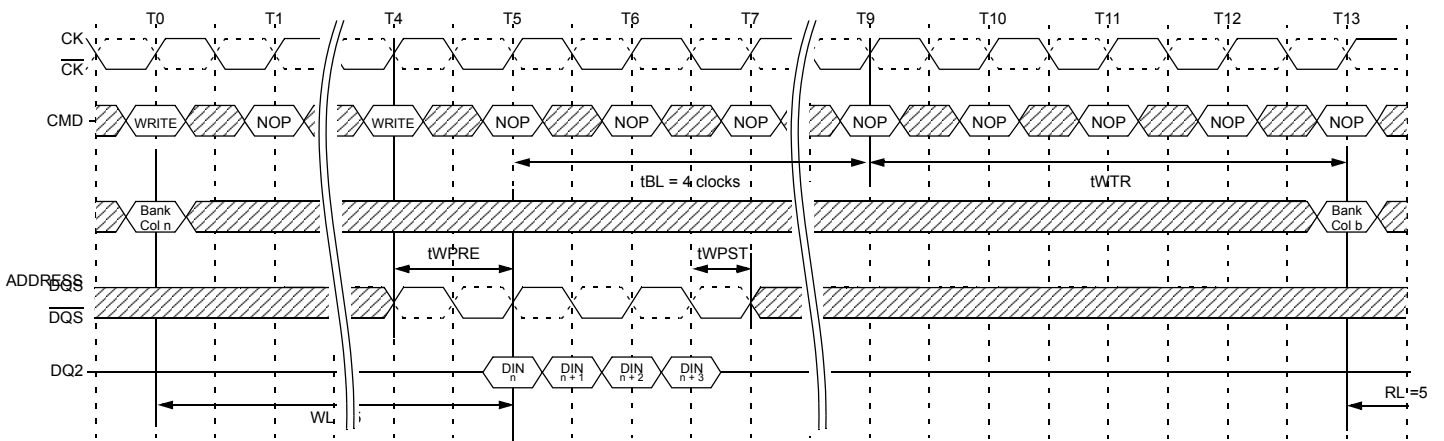
- NOTE :**
1. BC4, WL = 5(CWL = 5, AL = 0)
 2. DIN n (or b) = data-in from column n (or column b.)
 3. NOP commands are shown for ease of illustration ; other commands may be valid at these times.
 4. BC4 setting activated by MR0[A1:0=01] and A12 = 0 during WRITE commands at T0 and T4
 5. BC4 setting activated by MR0[A1:0=01] and A12 = 0 during WRITE commands at T0 and T4

Figure 50. WRITE (BC4) to WRITE (BC4) OTF



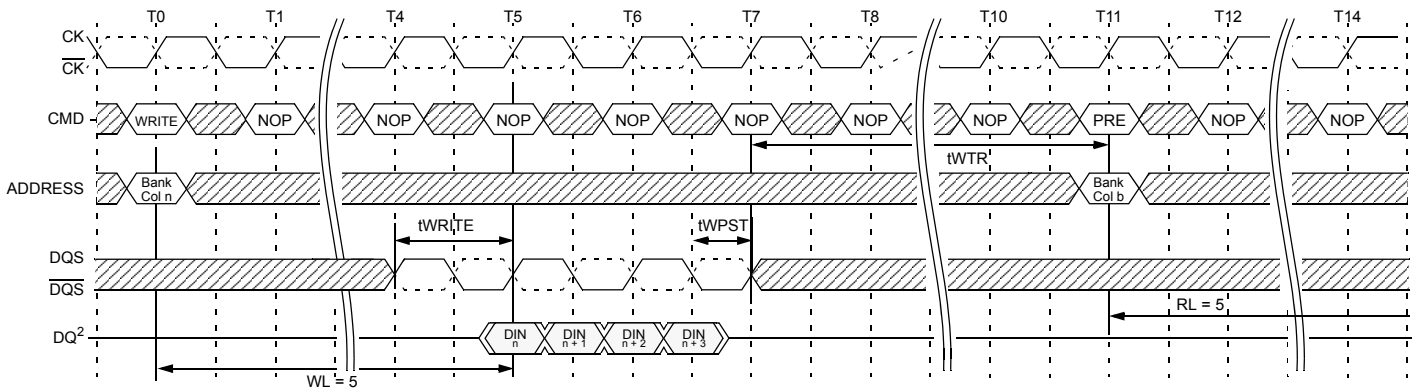
- NOTE :**
1. RL = 5 (CL = 5, AL = 0), WL = 5 (CWL = 5, AL = 0)
 2. DIN n = data-in from column n DOUT = data-in from column b.
 3. NOP commands are shown for ease of illustration ; other commands may be valid at these times.
 4. BL8 setting activated by either MR0[A1:0=00] or MR0[A1:0=01] and A12 = 1 during WRITE commands at T0. READ command at T11 can be either BC4 or BL8 depending on MR0[A1 : 0] and A12 status at T13.

Figure 51. WRITE (BL8) to READ (BC4/BL8)OTF



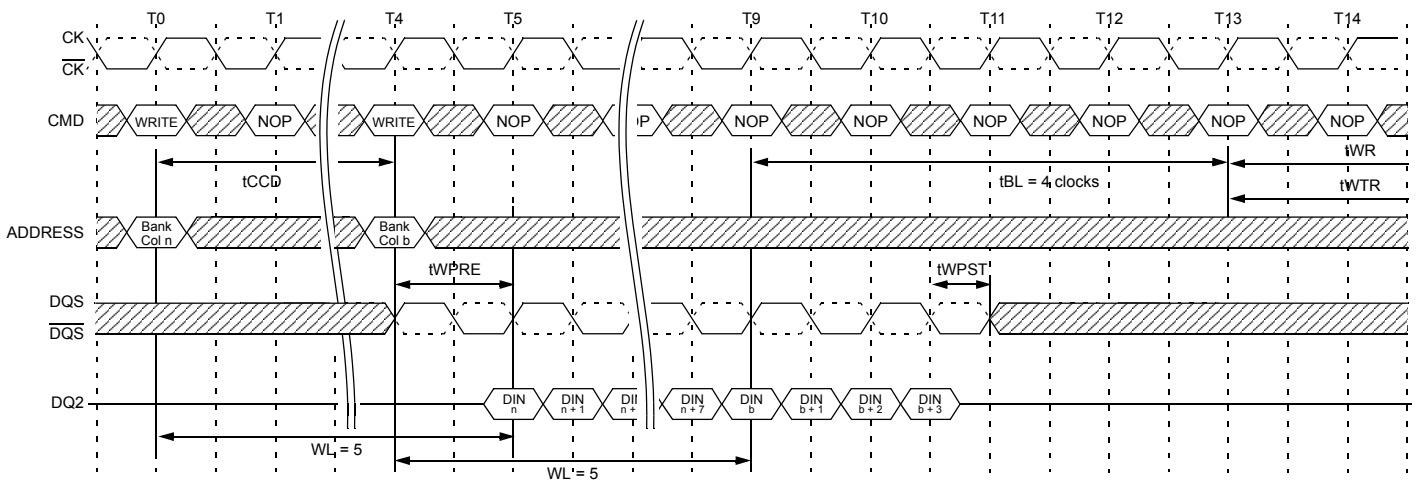
- NOTE :**
1. RL = 5 (CL = 5, AL = 0), WL = 5 (CWL =5, AL = 0)
 2. DIN n = data-in from column n; DOUT b = data-out from column b.
 3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
 4. BC4 setting activated by MR0[A1:0 = 01] and A12 = 0 during WRITE command at T0. READ command at T11 can be either BC4 or BL8 depending on A12 status at T13.

Figure 52. WRITE (BC4) to READ (BC4/BL8) OTF



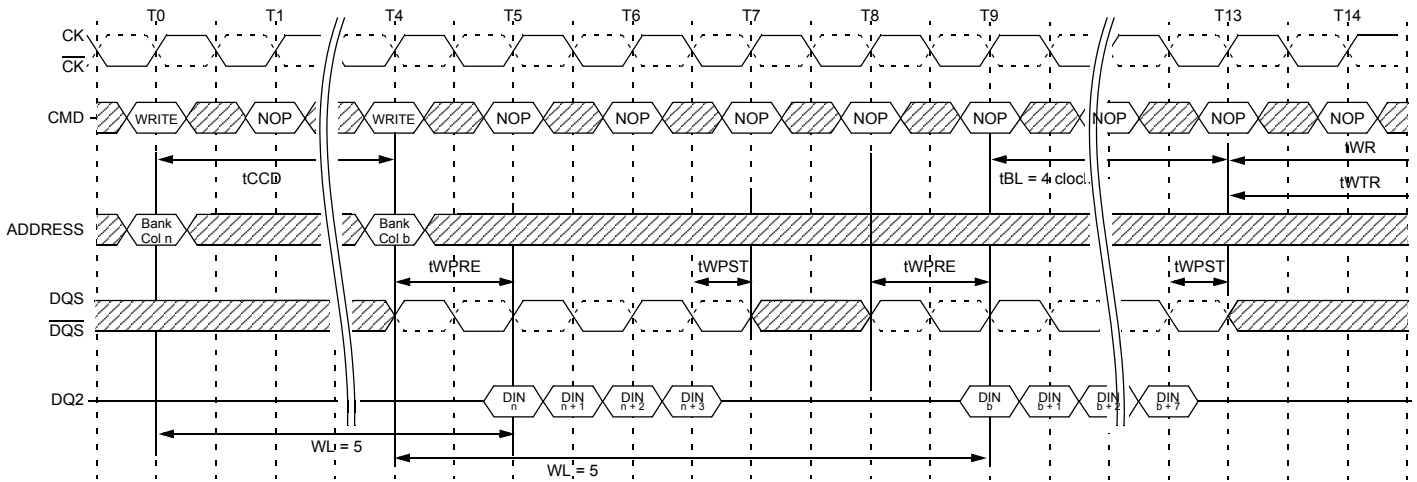
- NOTE :**
1. RL = 5 (CL = 5, AL = 0), WL = 5 (CWL =5, AL = 0)
 2. DIN n = data-in from column n; DOUT b = data-out from column b.
 3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
 4. BC4 setting activated by MR0[A1:0 = 10].

Figure 53. WRITE (BC4) to READ (BC4)



- NOTE :**
1. WL = 5 (CWL = 5, AL = 0)
 2. DIN n (or b) = data-in from column n (or column b).
 3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
 4. BL8 setting activated by MR0[A1:0 = 01] and A12 = 1 during WRITE command at T0.
BC4 setting activated by MR0[A1:0 = 01] and A12 = 0 during WRITE command at T4.

Figure 54. WRITE (BL8) to WRITE (BC4) OTF



- NOTE :**
1. WL = 5 (CWL = 5, AL = 0)
 2. DIN n (or b) = data-in from column n (or column b).
 3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
 4. BC4 setting activated by MR0[A1:0 = 01] and A12 = 0 during WRITE command at T0.
BL8 setting activated by MR0[A1:0 = 01] and A12 = 1 during WRITE command at T4.

Figure 55. WRITE (BC4) to WRITE (BL8) OTF

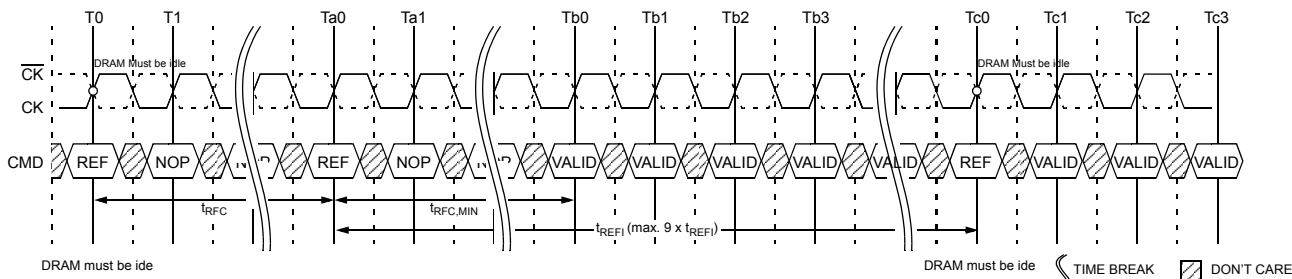
2.15 Refresh Command

The Refresh command (REF) is used during normal operation of the DDR3 SDRAMs. This command is non persistent, so it must be issued each time a refresh is required. The DDR3 SDRAM requires Refresh cycles at an average periodic interval of t_{REFI} . When \overline{CS} , \overline{RAS} and \overline{CAS} are held Low and \overline{WE} High at the rising edge of the clock, the chip enters a Refresh cycle. All banks of the SDRAM must be precharged and idle for a minimum of the precharge time $t_{RP}(\text{min})$ before the Refresh Command can be applied.

The refresh addressing is generated by the internal refresh controller. This makes the address bits "Don't Care" during a Refresh command. An internal address counter supplies the addresses during the refresh cycle. No control of the external address bus is required once this cycle has started.

When the refresh cycle has completed, all banks of the SDRAM will be in the precharged (idle) state. A delay between the Refresh Command and the next valid command, except NOP or DES, must be greater than or equal to the minimum Refresh cycle time $t_{RFC}(\text{min})$. Note that the t_{RFC} timing parameter depends on memory density.

In general, a Refresh command needs to be issued to the DDR3 SDRAM regularly every t_{REFI} interval. To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of 8 Refresh commands can be postponed during operation of the DDR3 SDRAM, meaning that at no point in time more than a total of 8 Refresh commands are allowed to be postponed. In case that 8 Refresh commands are postponed in a row, the resulting maximum interval between the surrounding Refresh commands is limited to $9 \times t_{REFI}$ (see Figure 57). A maximum of 8 additional Refresh commands can be issued in advance ("pulled in"), with each one reducing the number of regular Refresh commands required later by one. Note that pulling in more than 8 Refresh commands in advance does not further reduce the number of regular Refresh commands required later, so that the resulting maximum interval between two surrounding Refresh commands is limited to $9 \times t_{REFI}$ (see Figure 58). At any given time, a maximum of 16 REF commands can be issued within $2 \times t_{REFI}$. Self-refresh Mode may be entered with a maximum of eight Refresh commands being postponed. After exiting Self-Refresh Mode with one or more Refresh commands postponed, additional Refresh commands may be postponed to the extent that the total number of postponed Refresh commands (before and after the Self-Refresh) will never exceed eight.



NOTE :

1. Only NOP/DES commands allowed after Refresh command registered until $t_{RFC}(\text{min})$ expires.
2. Time interval between two Refresh commands may be extended to a maximum of $9 \times t_{REFI}$

Figure 56. Refresh Command Timing

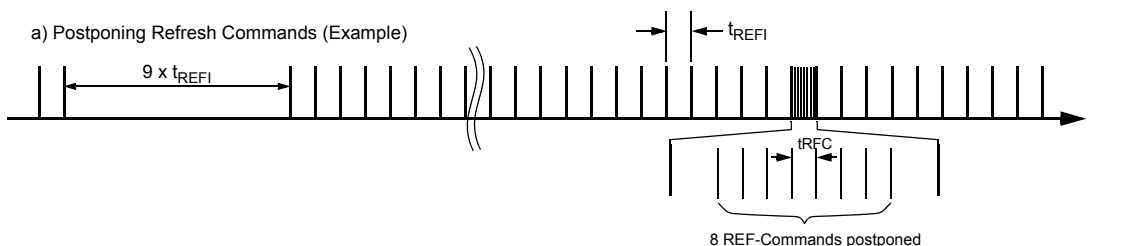


Figure 57. Postponing Refresh - Commands (Example)

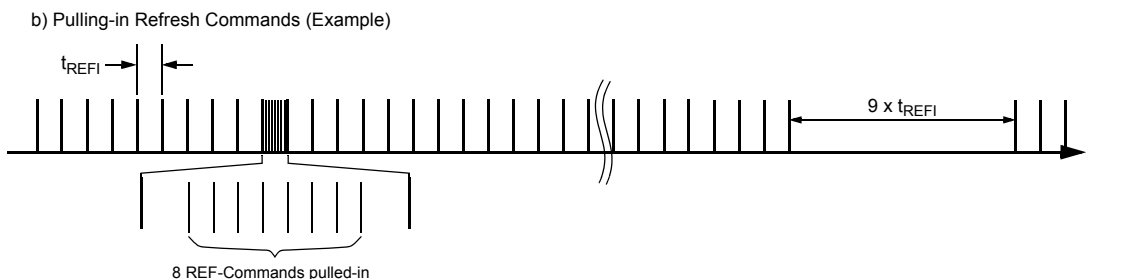


Figure 58. Pulling-in Refresh-Commands (Example)

2.16 Self-Refresh Operation

The Self-Refresh command can be used to retain data in the DDR3 SDRAM, even if the rest of the system is powered down. When in the Self-Refresh mode, the DDR3 SDRAM retains data without external clocking. The DDR3 SDRAM device has a built-in timer to accommodate Self-Refresh operation. The Self-Refresh-Entry (SRE) Command is defined by having \overline{CS} , \overline{RAS} , \overline{CAS} , and \overline{WE} held low with \overline{WE} high at the rising edge of the clock.

Before issuing the Self-Refresh-Entry command, the DDR3 SDRAM must be idle with all bank precharge state with t_{RP} satisfied. Also, on-die termination must be turned off before issuing Self-Refresh-Entry command, by either registering ODT pin low "ODTL + 0.5tCK" prior to the Self-Refresh Entry command or using MRS to MR1 command. Once the Self-Refresh Entry command is registered, \overline{CKE} must be held low to keep the device in Self-Refresh mode. During normal operation (DLL on), MR1(A0 = 0), the DLL is automatically disabled upon entering Self-Refresh and is automatically enabled (including a DLL-Reset) upon exiting Self-Refresh.

When the DDR3 SDRAM has entered Self-Refresh mode, all of the external control signals, except \overline{CKE} and \overline{RESET} , are "don't care". For proper Self-Refresh operation, all power supply and reference pins (VDD, VDDQ, VSS, VSSQ, VRefCA and VRefDQ) must be at valid levels. VrefDQ supply may be turned OFF in system during Self Refresh operation, provided that VrefDQ is valid and stable prior to \overline{CKE} going back High and that first Write operation may not occur earlier than 512nCK after exit from Self Refresh.

The DRAM initiates a minimum of one Refresh command internally within tCKE period once it enters Self-Refresh mode.

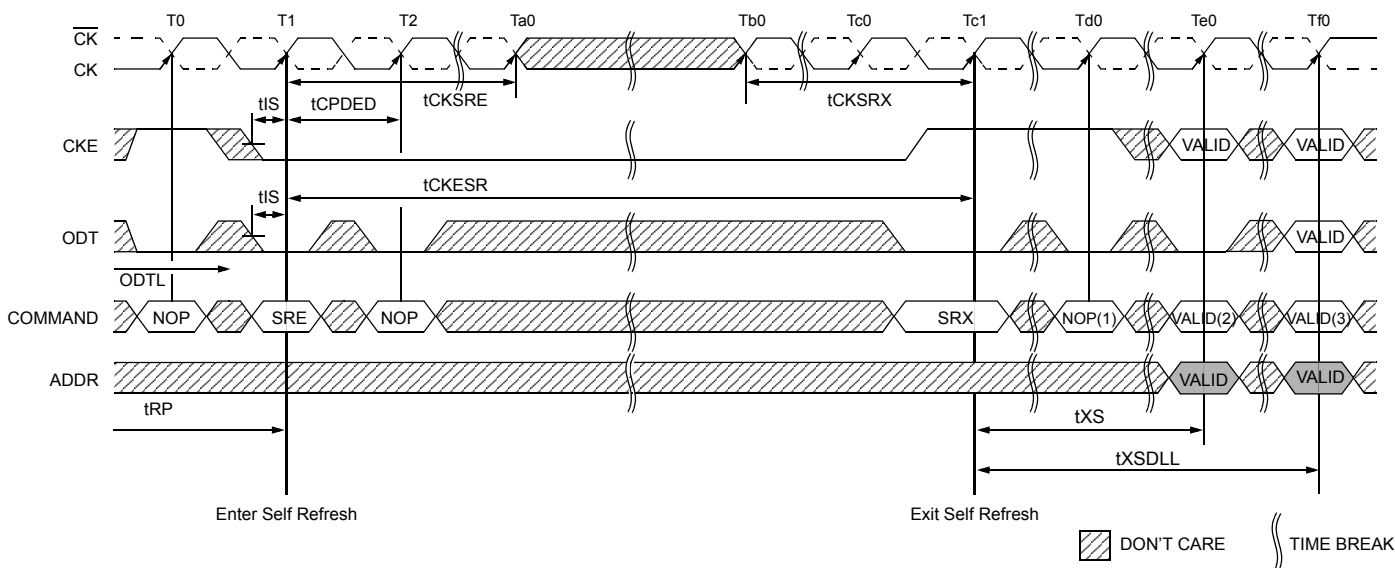
The clock is internally disabled during Self-Refresh Operation to save power. The minimum time that the DDR3 SDRAM must remain in Self-Refresh mode is tCKE. The user may change the external clock frequency or halt the external clock tCKSRE after Self-Refresh entry is registered, however, the clock must be restarted and stable tCKSRX before the device can exit Self-Refresh operation.

The procedure for exiting Self-Refresh requires a sequence of events. First, the clock must be stable prior to \overline{CKE} going back HIGH. Once a Self-Refresh Exit command (SRX, combination of \overline{CKE} going high and either NOP or Deselect on command bus) is registered, a delay of at least tXS must be satisfied before a valid command not requiring a locked DLL can be issued to the device to allow for any internal refresh in progress. Before a command which requires a locked DLL can be applied, a delay of at least tXSDLL and applicable ZQCAL function requirements (TBD) must be satisfied.

Before a command that requires a locked DLL can be applied, a delay of at least tXSDLL must be satisfied. Depending on the system environment and the amount of time spent in Self-Refresh, ZQ calibration commands may be required to compensate for the voltage and temperature drift as described in "ZQ Calibration Commands" on page 57. To issue ZQ calibration commands, applicable timing requirements must be satisfied (See Figure 73, "ZQ Calibration Timing", on page 57)

\overline{CKE} must remain HIGH for the entire Self-Refresh exit period tXSDLL for proper operation except for Self-Refresh re-entry. Upon exit from Self-Refresh, the DDR3 SDRAM can be put back into Self-Refresh mode after waiting at least tXS period and issuing one refresh command (refresh period of tRFC). NOP or deselect commands must be registered on each positive clock edge during the Self-Refresh exit interval tXS. ODT must be turned off during tXS-DLL.

The use of Self-Refresh mode introduces the possibility that an internally timed refresh event can be missed when \overline{CKE} is raised for exit from Self-Refresh mode. Upon exit from Self-Refresh, the DDR3 SDRAM requires a minimum of one extra refresh command before it is put back into Self-Refresh Mode.



- NOTE :**
1. Only NOP or DES commands
 2. Valid commands not requiring a locked DLL
 3. Valid commands requiring a locked DLL

Figure 59. Self-Refresh Entry/Exit Timing

2.17 Power-Down Modes

2.17.1 Power-Down Entry and Exit

Power-down is synchronously entered when CKE is registered low (along with NOP or Deselect command). CKE is not allowed to go low while mode register set command, MPR operations, ZQCAL operations, DLL locking or read / write operation are in progress. CKE is allowed to go low while any of other operations such as row activation, precharge or auto-precharge and refresh are in progress, but power-down IDD spec will not be applied until finishing those operations. Timing diagrams are shown in Figure 60 through Figure 72 with details for entry and exit of Power-Down.

The DLL should be in a locked state when power-down is entered for fastest power-down exit timing. If the DLL is not locked during power-down entry, the DLL must be reset after exiting power-down mode for proper read operation and synchronous ODT operation. DRAM design provides all AC and DC timing and voltage specification as well proper DLL operation with any CKE intensive operations as long as DRAM controller complies with DRAM specifications.

During Power-Down, if all banks are closed after any in progress commands are completed, the device will be in precharge Power-Down mode; if any bank is open after in progress commands are completed, the device will be in active Power-Down mode.

Entering power-down deactivates the input and output buffers, excluding CK, \overline{CK} , ODT, CKE and \overline{RESET} . To protect DRAM internal delay on CKE line to block the input signals, multiple NOP or Deselect commands are needed during the CKE switch off and cycle(s) after, this timing period are defined as tCPDED. CKE_low will result in deactivation of command and address receivers after tCPDED has expired.

[Table 13] Power-Down Entry Definitions

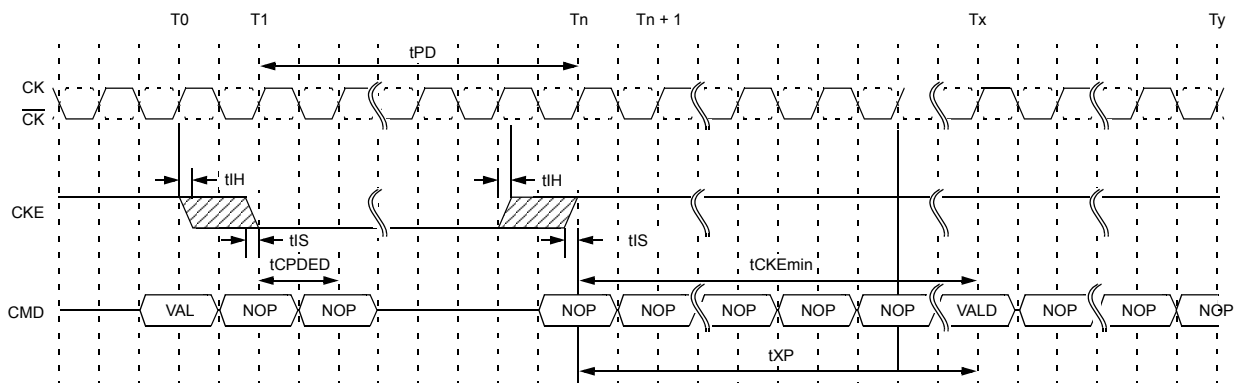
Status of DRAM	MRS bit A12	DLL	PD Exit	Relevant Parameters
Active (A bank or more Open)	Don't Care	On	Fast	tXP to any valid command
Pre Charged (All banks Precharged)	0	Off	Slow	tXP to any valid command. Since it is in precharge state, commands here will be ACT, AR, MRS/EMRS, PR or PRA tXPDLL to commands who need DLL to operate, such as RD, RDA or ODT control line.
Pre Charged (All Banks Precharged)	1	On	Fast	tXP to any valid command

Also, the DLL is disabled upon entering precharge power-down (Slow Exit Mode), but the DLL is kept enabled during precharge power-down (Fast Exit Mode) or active power-down. In power-down mode, CKE low, \overline{RESET} high and a stable clock signal must be maintained at the inputs of the DDR3 SDRAM, and ODT should be in a valid state but all other input signals are "Don't Care" (If \overline{RESET} goes low during Power-Down, the DRAM will be out of PD mode and into reset state.) CKE low must be maintained until tCKE has been satisfied. Power-down duration is limited by 9 times tREFI of the device.

The power-down state is synchronously exited when CKE is registered high (along with a NOP or Deselect command).

CKE high must be maintained until tCKE has been satisfied. A valid, executable command can be applied with power-down exit latency, tXP and/or tXP-DLL after CKE goes high. Power-down exit latency is defined at AC spec table of component data sheet.

Active Power Down Entry and Exit timing diagram example is shown in Figure 60. Timing Diagrams for CKE with PD Entry, PD Exit with Read and Read with Auto Precharge, Write, Write with Auto Precharge, Activate, Precharge, Refresh, and MRS are shown in Figure 61 through Figure 69. Additional clarifications are shown in Figure 70 through Figure 72.



NOTE : VAL command at T0 is ACT, NOP, DES or Precharge with still one bank remaining open after completion of precharge command.

Figure 60. Active Power-Down Entry and Exit Timing Diagram

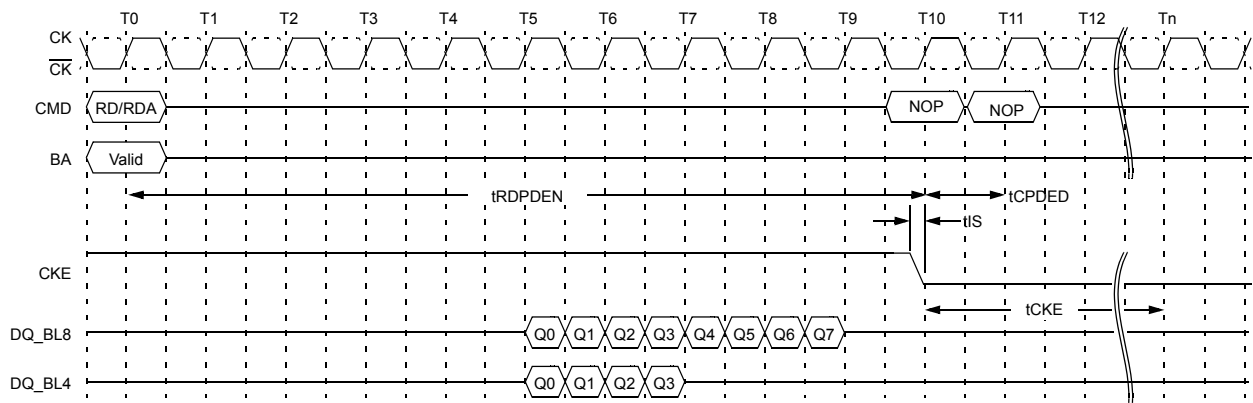


Figure 61. Power-Down Entry after Read and Read with Auto Precharge

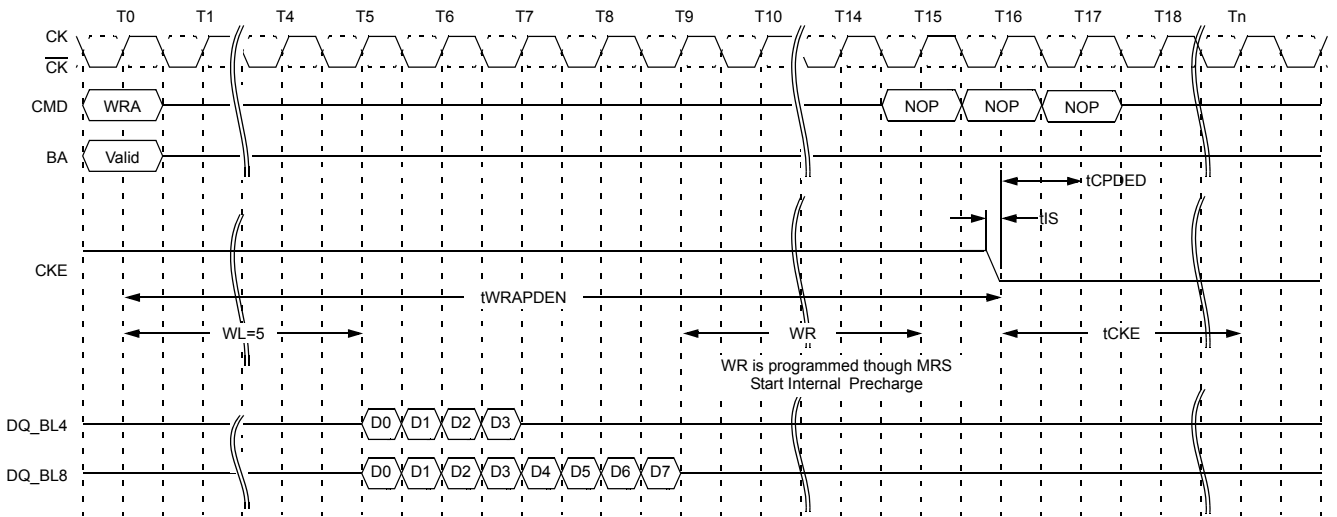


Figure 62. Power-Down Entry After Write with Auto Precharge

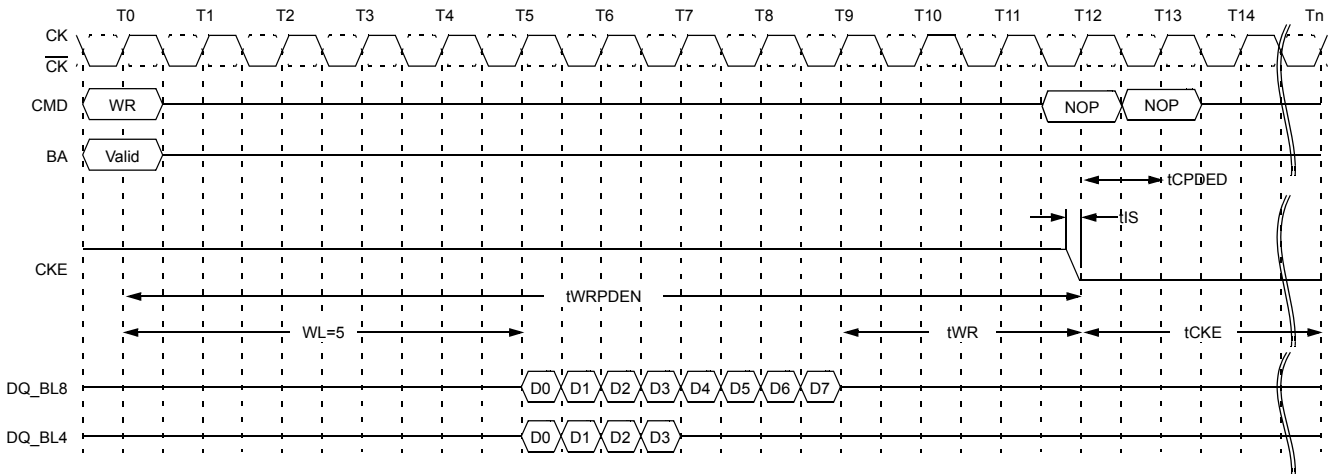


Figure 63. Power-Down Entry after Write

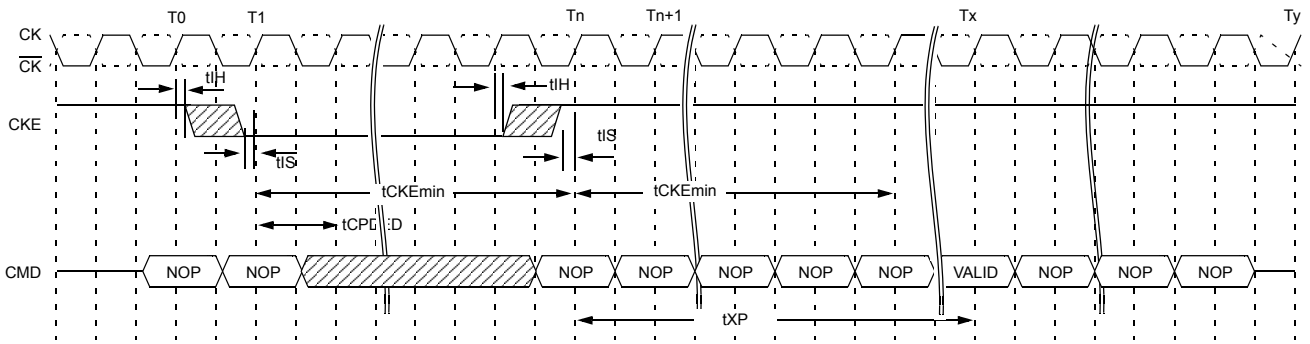


Figure 64. Precharge Power-Down (Fast Exit Mode) Entry and Exit

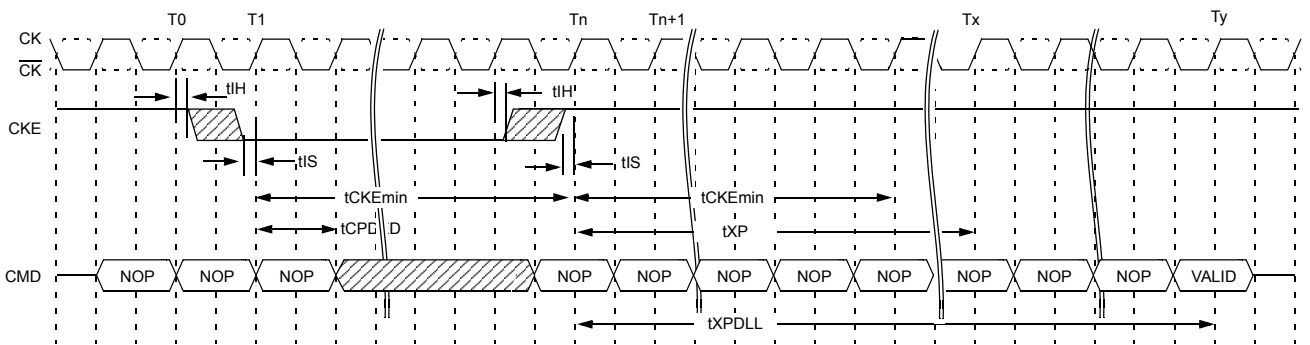


Figure 65. Precharge Power-Down (Slow Exit Mode) Entry and Exit

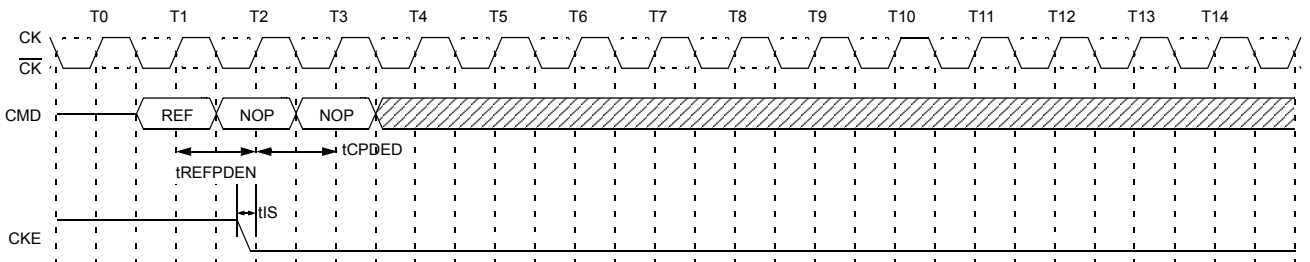


Figure 66. Refresh Command to Power-Down Entry

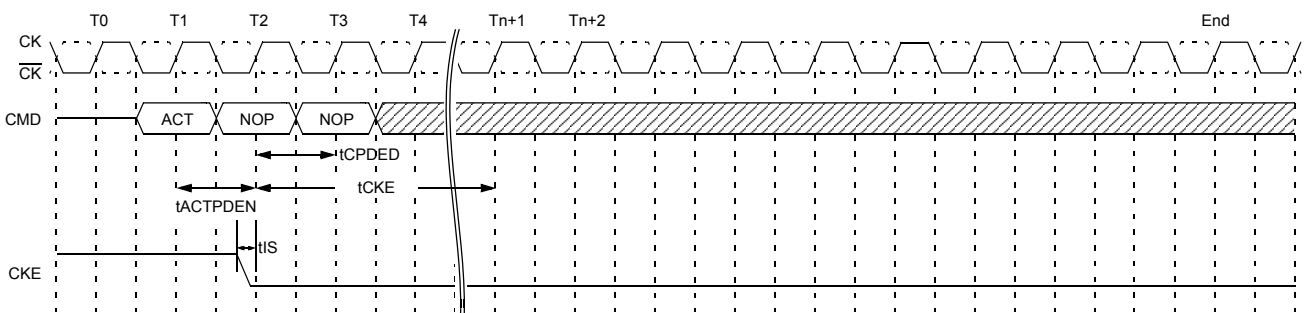


Figure 67. Active Command to Power-Down Entry

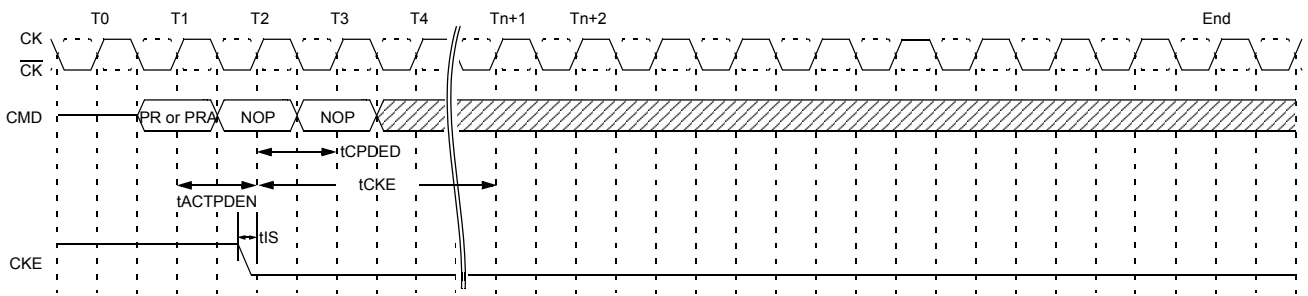


Figure 68. Precharge/Precharge all Command to Power-Down Entry

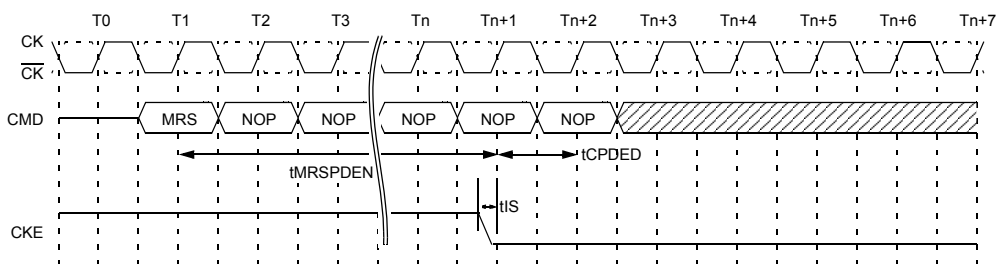
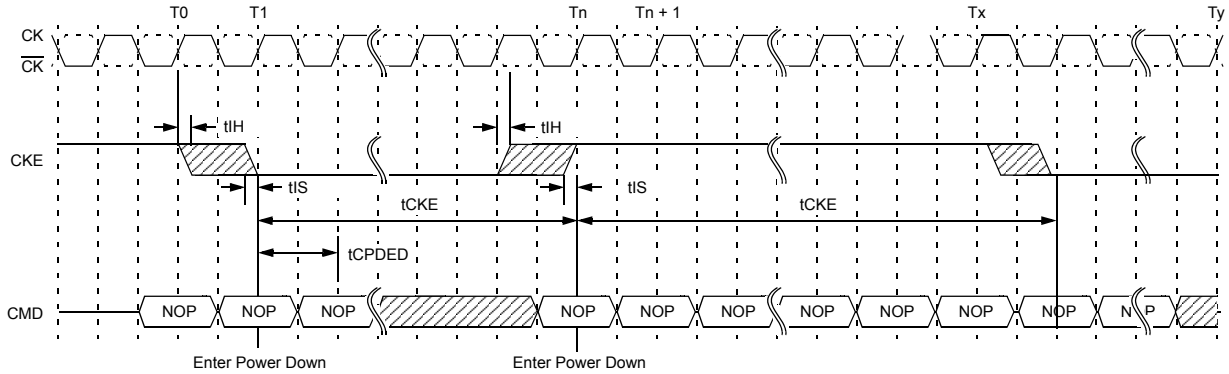


Figure 69. MRS Command to Power-Down Entry

2.17.2 Power-Down clarifications - Case 1

When CKE is registered low for power-down entry, $t_{PD(min)}$ must be satisfied before CKE can be registered high for power-down exit. The minimum value of parameter $t_{PD(min)}$ is equal to the minimum value

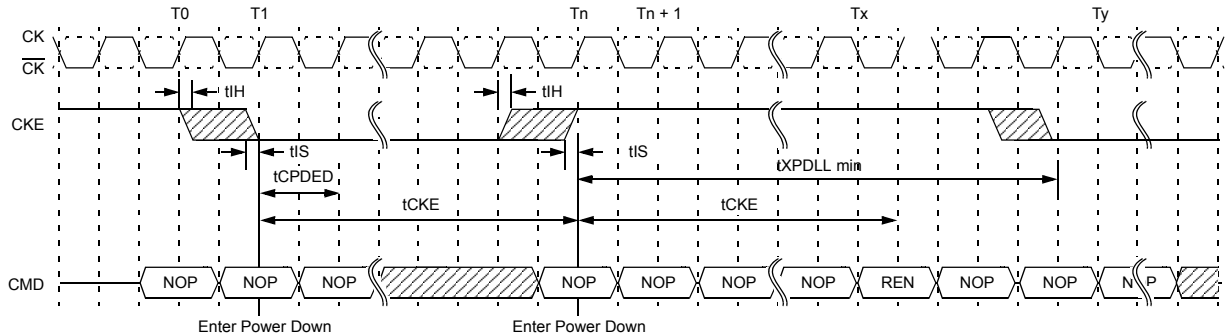


CASE 1 :
When CKE registered low for PD Entry, t_{CKE} must be satisfied before CKE can be registered high as PD Exit
CASE 1a :
After PD Exit, t_{CKE} must be satisfied before CKE can be registered low again.

Figure 70. Power-Down Entry/Exit Clarifications - Case1

2.17.3 Power-Down clarifications - Case 2

For certain CKE intensive operations, for example, repeated 'PD Exit - Refresh - PD Entry' sequence, the number of clock cycles between PD Exit and PD Entry may be insufficient to keep the DLL updated. Therefore the following conditions must be met in addition to t_{CKE} in order to maintain proper DRAM operation when the Refresh command is issued between PD Exit and PD Entry. Power-down mode can be used in conjunction with the Refresh command if the following conditions are met: 1) t_{XP} must be satisfied before issuing the command. 2) t_{XPDLL} must be satisfied (referenced to the registration of PD Exit) before the next power-down can be entered. A detailed example of Case 2 is shown in Figure 71.



CASE 2 :
For certain CKE intensive operations, for example, repeated "PD Exit - Refresh - PD Entry" sequence, the number of clock cycles between PD Exit and PD Entry may be insufficient to keep the DLL updated. Therefore the following conditions must be met in addition to t_{CKE} in order to maintain proper DRAM operation when Refresh command is issued in between PD Exit and PD Entry.

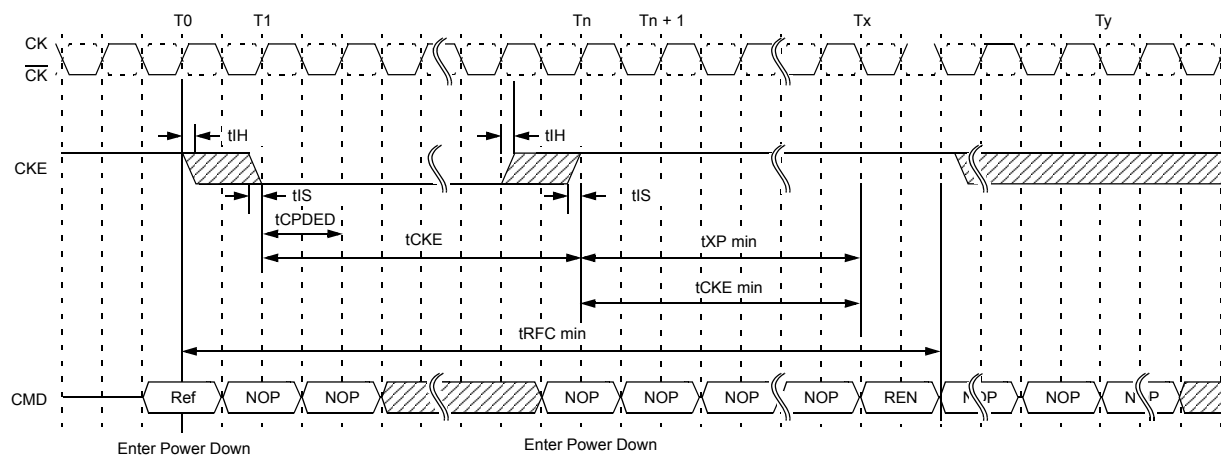
Power down mode can be used in conjunction with Refresh command if the following conditions are met:

1. t_{XP} must be satisfied before issuing the command
2. t_{XPDLL} must be satisfied (referenced to registration of PD exit) before next power down can be entered.

Figure 71. Power-Down Entry/Exit Clarifications - Case2

2.17.4 Power-Down clarifications - Case 3

If an early PD Entry is issued after a Refresh command, once PD Exit is issued, NOP or DES with CKE High must be issued until $t_{RFC}(\text{min})$ from the Refresh command is satisfied. This means CKE can not be registered low twice within a $t_{RFC}(\text{min})$ window. A detailed example of Case 3 is shown in Figure 72.



CASE 3 :

If an early PD Entry is issued after Refresh command, once PD Exit is issued, NOP or DES with CKE High must be issued until t_{RFC} from the Refresh command is satisfied. This means CKE can not be registered low twice within t_{RFC} window.

Figure 72. Power-Down Entry/Exit Clarifications - Case3

2.18 ZQ Calibration Commands

2.18.1 Calibration Description

ZQ Calibration command is used to calibrate DRAM Ron & ODT values over PVT. DDR3 SDRAM needs longer time to calibrate Ron & ODT at initialization and relatively smaller time to perform periodic calibrations.

ZQCL command is used to perform the initial calibration during power-up initialization sequence. This command may be issued at any time by the controller depending on the system environment. ZQCL command triggers the calibration engine inside the DRAM and once calibration is achieved the calibrated values are transferred from calibration engine to DRAM IO which gets reflected as updated Output Driver and ODT values.

The first ZQCL command issued after reset is allowed a timing period of tZQinit to perform the full calibration and the transfer of values. All other ZQCL commands except the first ZQCL command issued after RESET is allowed a timing period of tZQoper.

ZQCS command is used to perform periodic calibrations to account for VT variations. A shorter timing window is provided to perform the calibration and transfer of values as defined by timing parameter tZQCS. One ZQCS command can effectively correct a minimum of 0.5 % (ZQCorrection) of RON and RTT impedance error within 64 nCK for all speed bins assuming the maximum sensitivities specified in the 'Output Driver Voltage and Temperature Sensitivity' and 'ODT Voltage and Temperature Sensitivity' tables. The appropriate interval between ZQCS commands can be determined from these tables and other application-specific parameters. One method for calculating the interval between ZQCS commands, given the temperature (Tdribrate) and voltage (Vdribrate) drift rates that the SDRAM is subject to in the application, is illustrated. The interval could be defined by the following formula:

$$\text{ZQCorrection} = \frac{0.5}{(\text{TSens} \times \text{Tdribrate}) + (\text{VSens} \times \text{Vdribrate})}$$

where TSens = max(dRTTdT, dRONdTM) and VSens = max(dRTTdV, dRONdVM) define the SDRAM temperature and voltage sensitivities.

For example, if TSens = 1.5% / °C, VSens = 0.15% / mV, Tdribrate = 1 °C / sec and Vdribrate = 15 mV / sec, then the interval between ZQCS commands is calculated as:

$$\frac{0.5}{(1.5 \times 1) + (0.15 \times 15)} = 0.133 \approx 128\text{ms}$$

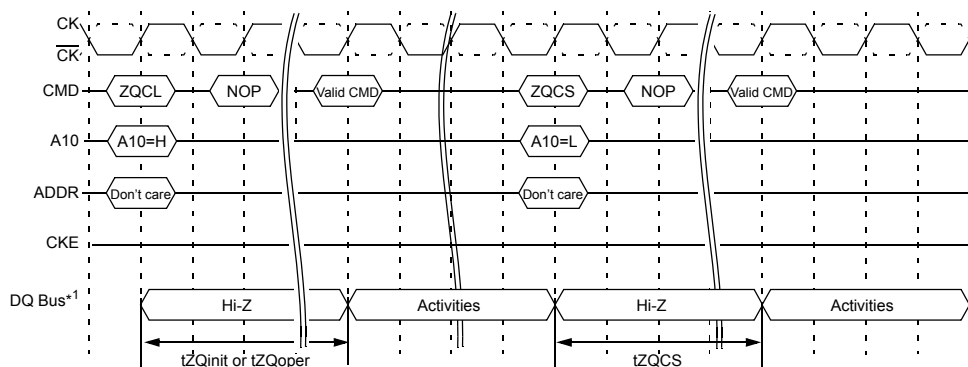
No other activities should be performed on the DRAM channel by the controller for the duration of tZQinit, tZQoper or tZQCS. The quiet time on the DRAM channel helps in accurate calibration of Ron and ODT. Once DRAM calibration is achieved, the DRAM should disable ZQ current consumption path to reduce power.

All banks must be precharged and tRP met before ZQCL or ZQCS commands are issued by the controller. See "[BA=Bank Address, RA=Row Address, CA=Column Address, BC#=Burst Chop, X=Don't Care, V=Valid]" on page 16 for a description of the ZQCL and ZQCS commands.

ZQ calibration commands can also be issued in parallel to DLL lock time when coming out of self refresh. Upon Self-Refresh exit, DDR3 SDRAM will not perform an IO calibration without an explicit ZQ calibration command. The earliest possible time for ZQ Calibration command (short or long) after self refresh exit is tXS.

In systems that share the ZQ resistor between devices, the controller must not allow any overlap of tZQoper or tZQinit or tZQCS between the devices.

2.18.2 ZQ Calibration Timing



NOTE : ODT must be disabled during calibration procedure
 *1: All devices connected to DQ bus should be high impedance during calibration

Figure 73. ZQ Calibration Timing

2.18.3 ZQ External Resistor Value and Tolerance and Capacitive loading

In order to use the ZQ Calibration function, a 240 ohm +/- 1% tolerance external resistor must be connected between the ZQ pin and ground. The single resistor can be used for each SDRAM or one resistor can be shared between two SDRAMs if the ZQ calibration timings for each SDRAM do not overlap. The total capacitive loading on the ZQ pin must be limited. (See "Input/Output Capacitance" on component datasheet)

3. On-Die Termination (ODT)

ODT (On-Die Termination) is a feature of the DDR3 SDRAM that allows the DRAM to turn on/off termination resistance for each DQ, DQS, \overline{DQS} and DM for x4 and x8 configuration (and TDQS, \overline{TDQS} for X8 configuration, when enabled via A11=1 in MR1) via the ODT control pin. For x16 configuration, ODT is applied to each DQU, DQL, DQSU, \overline{DQSU} , DQSL, \overline{DQSL} , DMU and DML signal via the ODT control pin. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices. More details about ODT control modes and ODT timing modes can be found further down in this document :

- The ODT control modes are described in 3.1.
- The ODT synchronous mode is described in 3.2
- The dynamic ODT feature is described in 3.3
- The ODT asynchronous mode is described in 3.4
- The transitions between ODT synchronous and asynchronous are described in 3.4.1 through 3.4.4

The ODT feature is turned off and not supported in Self-Refresh mode.
A simple functional representation of the DRAM ODT feature is shown in Figure 74.

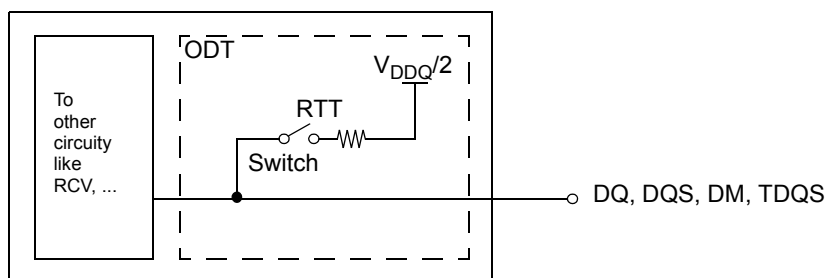


Figure 74. Functional Representation of ODT

The switch is enabled by the internal ODT control logic, which uses the external ODT pin and other control information, see below. The value of RTT is determined by the settings of Mode Register bits (see Figure 7 on page 11 and Figure 8 on page 14). The ODT pin will be ignored if the Mode Registers MR1 and MR2 are programmed to disable ODT and in self-refresh mode.

3.1 ODT Mode Register and ODT Truth Table

The ODT Mode is enabled if either of MR1 bits A2 or A6 or A9 are non zero. In this case, the value of RTT is determined by the settings of those bits (see Figure 7 on page 11).

- Application: Controller sends WR command together with ODT asserted.
- One possible application: The rank that is being written to provides termination.
 - DRAM turns ON termination if it sees ODT asserted (except ODT is disabled by MR).
 - DRAM does not use any write or read command decode information.
 - The Termination Truth Table is shown in Table 14.

[Table 14] Termination Truth Table

ODT pin	DRAM Termination State
0	OFF
1	ON, (OFF, if disabled by MR1 {A9, A6, A2} and MR2 {A10, A9} in general)

3.2 Synchronous ODT Mode

Synchronous ODT mode is selected whenever the DLL is turned on and locked. Based on the power-down definition, these modes are:

- Any bank active with CKE high
- Refresh with CKE high
- Idle mode with CKE high
- Active power down mode (regardless of MR0 bit A12)
- Precharge power down mode if DLL is enabled during precharge power down by MR0 bit A12.

The direct ODT feature is not supported during DLL-off mode. The on-die termination resistors must be disabled by continuously registering the ODT pin low and/or by programming the RTT_Nom bits MR1{A9,A6,A2} to {0,0,0} via a mode register set command during DLL-off mode.

In synchronous ODT mode, RTT will be turned on ODTLon clock cycles after ODT is sampled high by a rising clock edge and turned off ODTLoff clock cycles after ODT is registered low by a rising clock edge. The ODT latency is tied to the write latency (WL) by: $ODTLon = WL - 2$; $ODTLoff = WL - 2$.

3.2.1 ODT Latency and Posted ODT

In Synchronous ODT Mode, the Additive Latency (AL) programmed into the Mode Register (MR1) also applies to the ODT signal. The DRAM internal ODT signal is delayed for a number of clock cycles defined by the Additive Latency (AL) relative to the external ODT signal. $ODTLon = CWL + AL - 2$; $ODTLoff = CWL + AL - 2$. For details, refer to DDR3 SDRAM latency definitions.

[Table 15] ODT Latency

Symbol	Parameter	DDR3-800	DDR-1066	DDR3-1333	DDR3-1600	Unit
ODTLon	ODT turn on Latency	$WL - 2.0 = CWL + AL - 2.0$				tCK
ODTLoff	ODT turn on Latency	$WL - 2.0 = CWL + AL - 2.0$				

3.2.2 Timing Parameters

In synchronous ODT mode, the following timing parameters apply (see Figure 75 on page 60):

ODTLon, ODTLoff, tAON,min,max, tAOF,min,max.

Minimum RTT turn-on time (tAONmin) is the point in time when the device leaves high impedance and ODT resistance begins to turn on. Maximum RTT turn on time (tAONmax) is the point in time when the ODT resistance is fully on. Both are measured from ODTLon.

Minimum RTT turn-off time (tAOFmin) is the point in time when the device starts to turn off the ODT resistance.

Maximum RTT turn off time (tAOFmax) is the point in time when the on-die termination has reached high impedance.

Both are measured from ODTLoff.

When ODT is asserted, it must remain high until ODTH4 is satisfied. If a Write command is registered by the SDRAM with ODT high, then ODT must remain high until ODTH4 (BL = 4) or ODTH8 (BL = 8) after the Write command (see Figure 76 on page 60). ODTH4 and ODTH8 are measured from ODT registered high to ODT registered low or from the registration of a Write command until ODT is registered low.

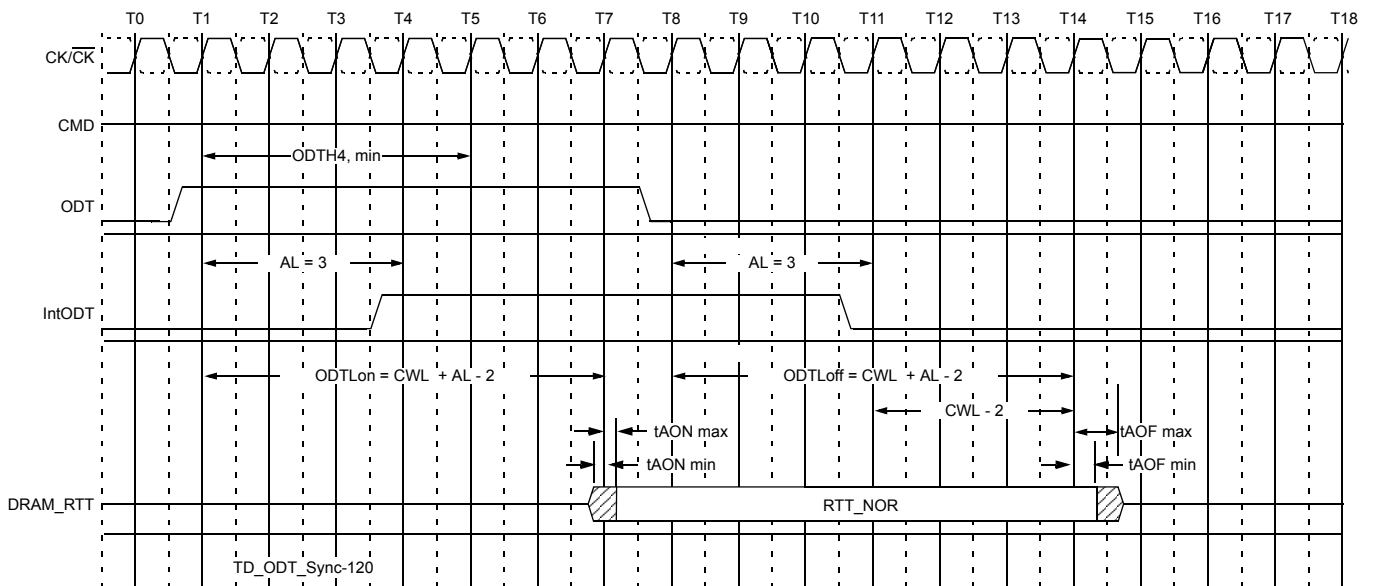


Figure 75. Synchronous ODT Timing Example for AL=3; CWL=5; ODTLon=AL+CWL-2=6.0; ODTLoft=AL+CWL-2=6

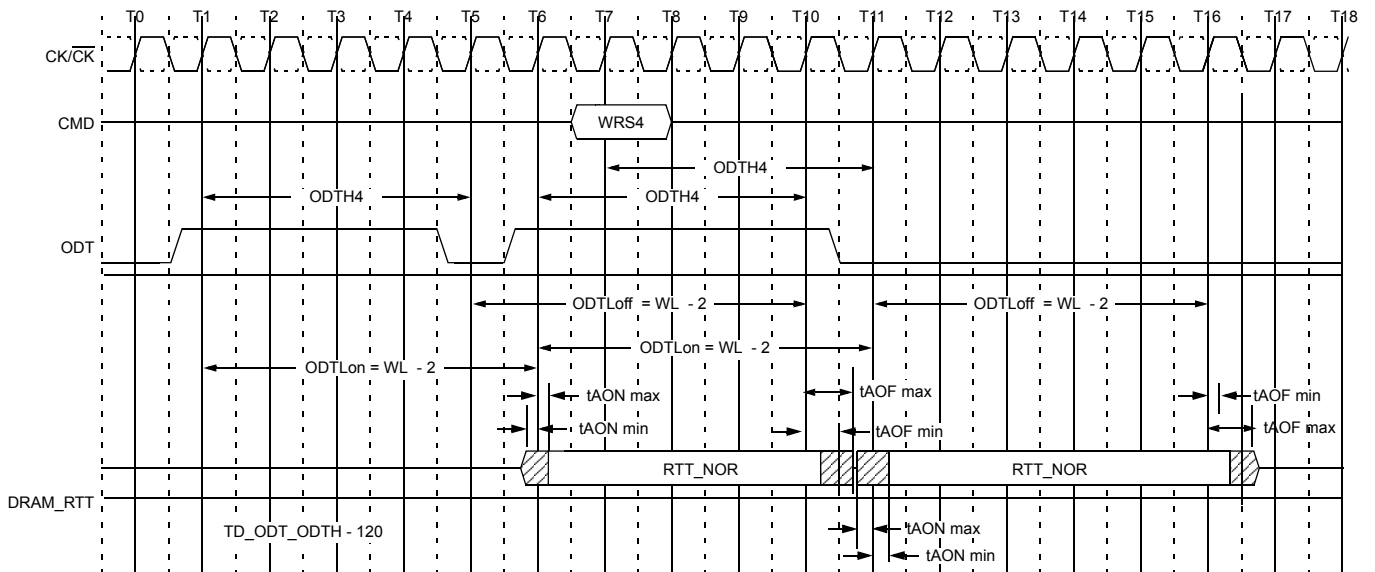


Figure 76. Synchronous ODT example with BL=4, WL=7

ODT must be held high for at least ODT_{H4} after assertion (T1); ODT must be kept high ODT_{H4} (BL = 4) or ODT_{H8} (BL = 8) after Write command (T7). ODT_H is measured from ODT first registered high to ODT first registered low, or from registration of Write command with ODT high to ODT registered low. Note that although ODT_{H4} is satisfied from ODT registered high at T6 ODT must not go low before T11 as ODT_{H4} must also be satisfied from the registration of the Write command at T7.

3.2.3 ODT during Reads:

As the DDR3 SDRAM can not terminate and drive at the same time, RTT must be disabled at least half a clock cycle before the read preamble by driving the ODT pin low appropriately. RTT may nominally not be enabled until one clock cycle after the end of the post-amble as shown in the example below. As shown in Figure 77 below at cycle T15, DRAM turns on the termination when it stops driving which is determined by t_{HZ}. If DRAM stops driving early (i.e t_{HZ} is early) than t_{AONmin} timing may apply. If DRAM stops driving late (i.e t_{HZ} is late) than DRAM complies with t_{AONmax} timing. Note that ODT may be disabled earlier before the Read and enabled later after the Read than shown in this example in Figure 77.

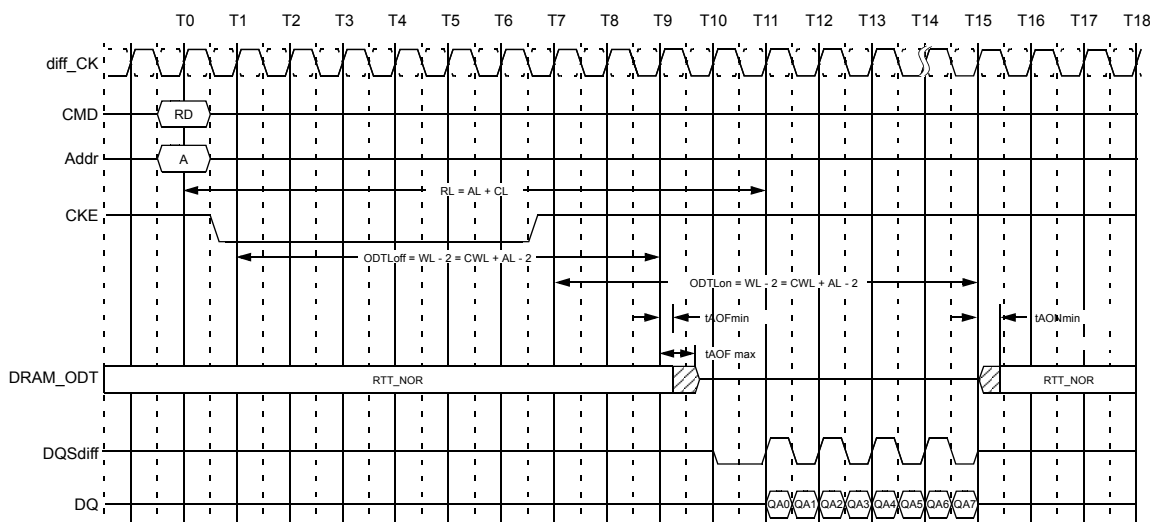


Figure 77. ODT must be disabled externally during Reads by driving ODT low.
 (example: CL=6; AL=CL-1=5; RL=AL+CL=11; CWL=5; ODTLon=CWL+AL-2=8; ODTLoff=CWL+AL-2=8)

3.3 Dynamic ODT

In certain application cases and to further enhance signal integrity on the data bus, it is desirable that the termination strength of the DDR3 SDRAM can be changed without issuing an MRS command. This requirement is supported by the "Dynamic ODT" feature as described as follows:

3.3.1 Functional Description:

The Dynamic ODT Mode is enabled if bit (A9) or (A10) of MR2 is set to '1'. The function is described as follows:

- Two RTT values are available: RTT_Nom and RTT_WR.
 - The value for RTT_Nom is preselected via bits A[9,6,2] in MR1
 - The value for RTT_WR is preselected via bits A[10,9] in MR2
- During operation without commands, the termination is controlled as follows;
 - Nominal termination strength RTT_Nom is selected.
 - Termination on/off timing is controlled via ODT pin and latencies ODTLon and ODTLoff.
- When a write command (WR, WRA, WRS4, WRS8, WRAS4, WRAS8) is registered, and if Dynamic ODT is enabled, the termination is controlled as follows:
 - A latency ODTLcnw after the write command, termination strength RTT_WR is selected.
 - A latency ODTLcwn8 (for BL8, fixed by MRS or selected OTF) or ODTLcwn4 (for BC4, fixed by MRS or selected OTF) after the write command, termination strength RTT_Nom is selected.
 - Termination on/off timing is controlled via ODT pin and ODTLon, ODTLoff.

Table 16 shows latencies and timing parameters which are relevant for the on-die termination control in Dynamic ODT mode.

The dynamic ODT feature is not supported at DLL-off mode. User must use MRS command to set Rtt_WR, MR2{A10,A9}={0,0}, to disable Dynamic ODT externally.

When ODT is asserted, it must remain high until ODTH4 is satisfied. If a Write command is registered by the SDRAM with ODT high, then ODT must remain high until ODTH4 (BL = 4) or ODTH8 (BL = 8) after the Write command (see Figure 76) ODTH4 and ODTH8 are measured from ODT registered high to ODT registered low or from the registration of a Write command until ODT is registered low.

[Table 16] Latencies and timing parameters relevant for Dynamic ODT

Name and Description	Abbr.	Defined from	Define to	Definition for all DDR3 speed bins	Unit
ODT turn-on Latency	ODTLon	registering external ODT signal high	turning termination on	ODTLon = WL - 2	tCK
ODT turn-off Latency	ODTLoff	registering external ODT signal low	turning termination off	ODTLoff = WL - 2	tCK
ODT Latency for changing from RTT_Nom to RTT_WR	ODTLcnw	registering external write command	change RTT strength from RTT_Nom to RTT_WR	ODTLcnw = WL - 2	tCK
ODT Latency for change from RTT_WR to RTT_Nom (BL = 4)	ODTLcwn4	registering external write command	change RTT strength from RTT_WR to RTT_Nom	ODTLcwn4 = 4 + ODTLoff	tCK
ODT Latency for change from RTT_WR to RTT_Nom (BL = 8)	ODTLcwn8	registering external write command	change RTT strength from RTT_WR to RTT_Nom	ODTLcwn8 = 6 + ODTLoff	tCK(avg)
minimum ODT hold time after ODT assertion	ODTH4	registering ODT high	ODT registered low	ODTH4 = 4	tCK(avg)
minimum ODT hold time after Write (BL = 4)	ODTH4	registering Write with ODT high	ODT registered low	ODTH4 = 4	tCK(avg)
minimum ODT hold time after Write (BL = 8)	ODTH8	registering Write with ODT high	ODT registered low	ODTH8 = 6	tCK(avg)
RTT change skew	tADC	ODTLcnw ODTLcwn	RTT valid	tADC(min) = 0.3 * tCK(avg) tADC(max) = 0.7 * tCK(avg)	tCK(avg)

NOTE : tAOF,nom and tADC,nom are 0.5 tCK (effectively adding half a clock cycle to ODTLoff, ODTcnw and ODTLcwn)

3.3.2 ODT Timing Diagrams

The following pages provide exemplary timing diagrams as described in Table 17:

[Table 17] Timing Diagrams for "Dynamic ODT"

Figure	Description
Figure 78	Dynamic ODT: Behavior with ODT being asserted before and after the write.
Figure 79	Dynamic ODT: Behavior without write command, AL = 0, CWL = 5.
Figure 80	Dynamic ODT: Behavior with ODT pin being asserted together with write command for a duration of 6 clock cycles.
Figure 81	Dynamic ODT: Behavior with ODT pin being asserted together with write command for a duration of 6 clock cycles, example for BC4 (via MRS or OTF), AL = 0, CWL = 5.
Figure 82	Dynamic ODT: Behavior with ODT pin being asserted together with write command for a duration of 4 clock cycles.

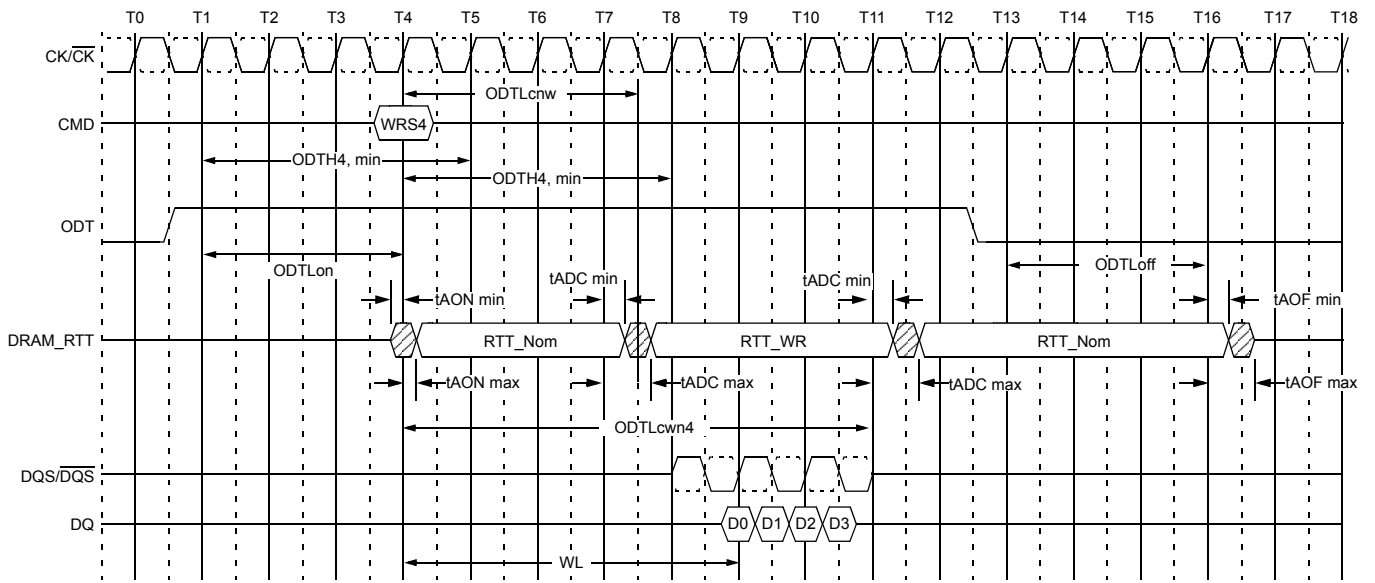


Figure 78. Dynamic ODT : Behavior with ODT being asserted before and after the write, example for BC4(via MRS or OTF), AL=0, CWL=5

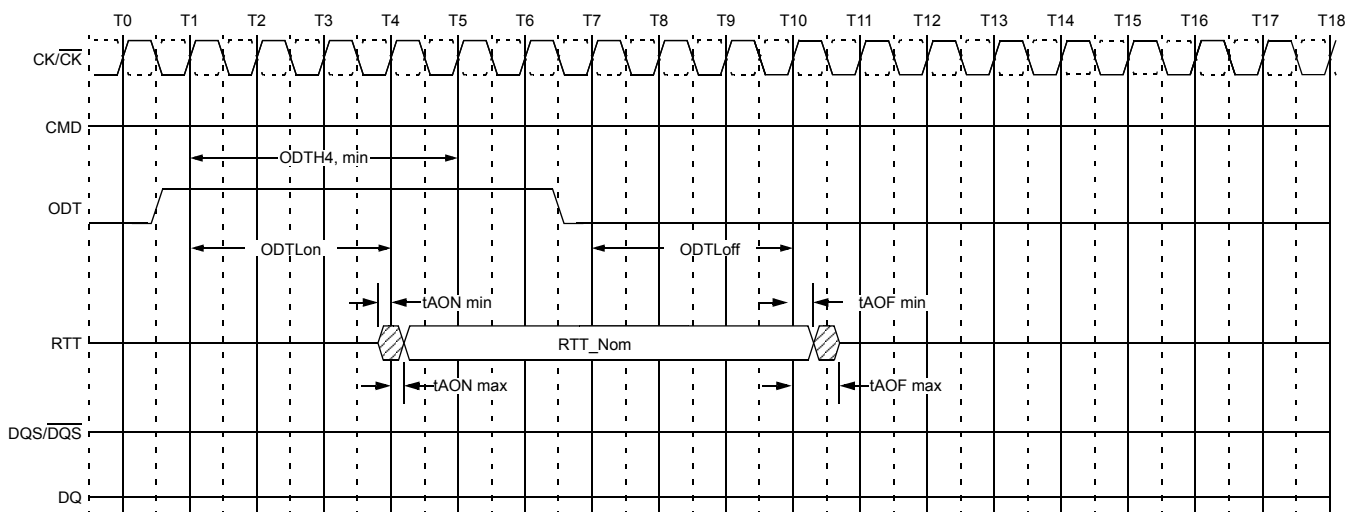


Figure 79. Dynamic ODT : Behavior without write command, AL=0, CWL=5

3.4 Asynchronous ODT mode

Asynchronous ODT mode is selected when DRAM runs in DLLon mode, but DLL is temporarily disabled (i.e. frozen) in precharge power-down (by MR0 bit A12). Based on the power down mode definitions, this is currently Precharge power down mode if DLL is disabled during precharge power down by MR0 bit A12.

In asynchronous ODT timing mode, internal ODT command is NOT delayed by Additive Latency (AL) relative to the external ODT command. In asynchronous ODT mode, the following timing parameters apply

$t_{AONPD,min,max}$, $t_{AOFPD,min,max}$

Minimum RTT turn-on time ($t_{AONPDmin}$) is the point in time when the device termination circuit leaves high impedance and ODT resistance begins to turn on. Maximum RTT turn on time ($t_{AONPDmax}$) is the point in time when the ODT resistance is fully on.

$t_{AONPDmin}$ and $t_{AONPDmax}$ are measured from ODT being sampled high.

Minimum RTT turn-off time ($t_{AOFPDmin}$) is the point in time when the devices termination circuit starts to turn off the ODT resistance. Maximum ODT turn off time ($t_{AOFPDmax}$) is the point in time when the on-die termination has reached high impedance. $t_{AOFPDmin}$ and $t_{AOFPDmax}$ are measured from ODT being sampled low.

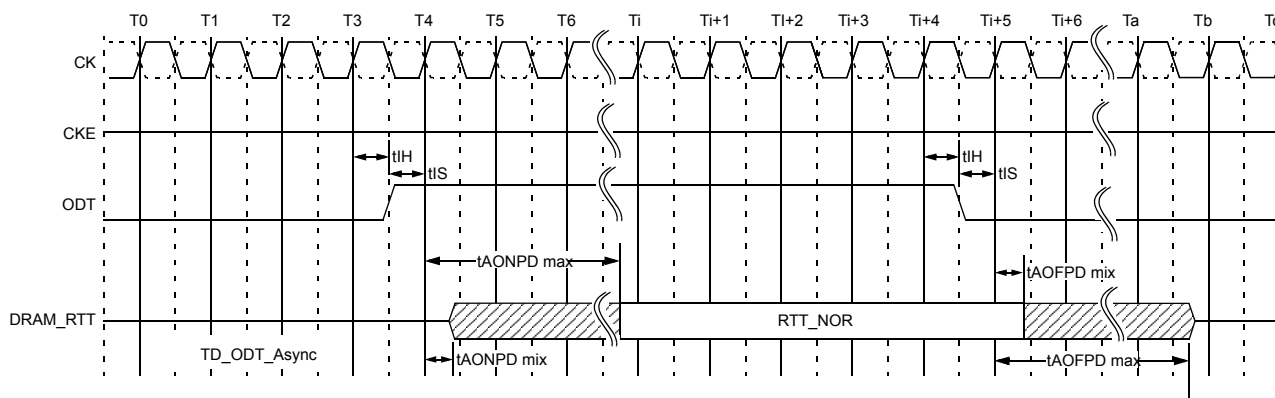


Figure 83. Asynchronous ODT Timing on DDR3 SDRAM with fast ODT transition: AL is ignored

In Precharge Power Down, ODT receiver remains active, however no Read or Write command can be issued, as the respective ADD/CMD receivers may be disabled.

[Table 18] Asynchronous ODT Timing Parameters for all Speed Bins

Symbol	Description	min	max	Unit
t_{AONPD}	Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	2	8.5	ns
t_{AOFPD}	Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	2	8.5	ns

3.4.1 Synchronous to Asynchronous ODT Mode Transition

[Table 19] ODT timing parameters for Power Down (with DLL frozen) entry and exit transition period

Description	min	max
ODT to RTT turn-on delay	$\min\{ODTLon * t_{CK} + t_{AONmin}; t_{AONPDmin}\}$	$\max\{ODTLon * t_{CK} + t_{AONmax}; t_{AONPDmax}\}$
	$\min\{(WL - 2.0) * t_{CK} + t_{AONmin}; t_{AONPDmin}\}$	$\max\{(WL - 2.0) * t_{CK} + t_{AONmax}; t_{AONPDmax}\}$
ODT to RTT turn-off delay	$\min\{ODTloff * t_{CK} + t_{AOFmin}; t_{AOFPDmin}\}$	$\max\{ODTloff * t_{CK} + t_{AOFmax}; t_{AOFPDmax}\}$
	$\min\{(WL - 2.0) * t_{CK} + t_{AOFmin}; t_{AOFPDmin}\}$	$\max\{(WL - 2.0) * t_{CK} + t_{AOFmax}; t_{AOFPDmax}\}$
t_{ANPD}	WL - 1	

3.4.2 Synchronous to Asynchronous ODT Mode Transition during Powerdown Entry

if DLL is selected to be frozen in Precharge Power Down Mode by the setting of bit A12 in MR0 to "0" there is a transition period around power down entry, where the DDR3 SDRAM may show either synchronous or asynchronous ODT behavior. This transition period ends when CKE is first registered low and starts t_{ANPD} before that. If there is a Refresh command in progress while CKE goes low, then the transition period ends t_{RFC} after the Refresh command. t_{ANPD} is equal to $(WL-1)$ and is counted (backwards) from the clock cycle where CKE is first registered low. The transition period begins with the starting point of t_{ANPD} and terminates at the end point of $t_{CPDED(min)}$ as shown in Figure 84. If there is a Refresh command in progress while CKE goes low, then the transition period ends at the later one of $t_{RFC(min)}$ after the Refresh command and the end point of $t_{CPDED(min)}$ as shown in Figure 85. Please note that the actual starting point at t_{ANPD} is excluded from the transition period, and the actual end point at $t_{CPDED(min)}$ and $t_{RFC(min)}$, respectively, are included in the transition period. ODT assertion during the transition period may result in an RTT change as early as the smaller of $t_{AONPD min}$ and $(ODT_{Lon} * t_{CK} + t_{AONmin})$ and as late as the larger of $t_{AONPD max}$ and $(ODT_{Loff} * t_{CK} + t_{AONmax})$. ODT de-assertion during the transition period may late as the larger of $t_{AOFPD max}$ and $(ODT_{Loff} * t_{CK} + t_{AOFmax})$. Note that, if AL has a large Value, the range where RTT is uncertain becomes quite large. it shows the three different cases: ODT_A, synchronous behavior before t_{ANPD} ; ODT_B has a state change during the transition period; ODT_C shows a state change after the transition period.

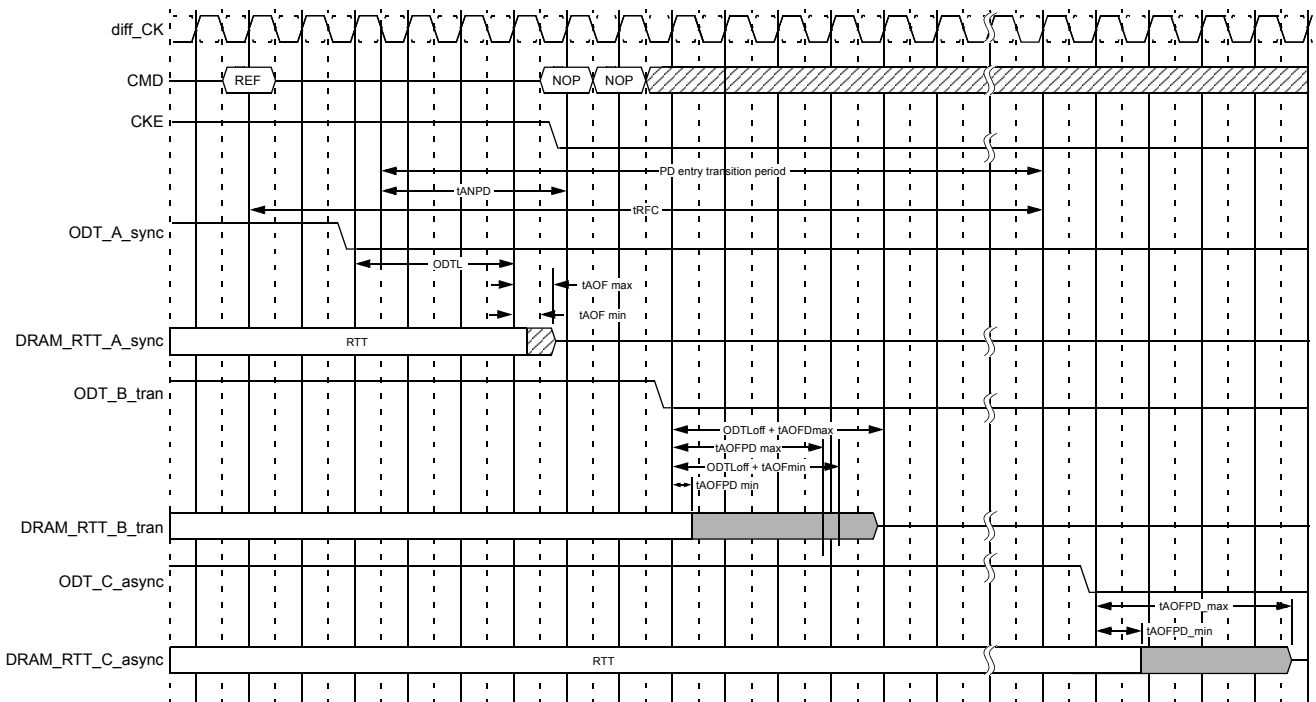


Figure 84. Synchronous to asynchronous transition after Refresh command (AL=0; CWL=5; tANPD=WL-1=4)

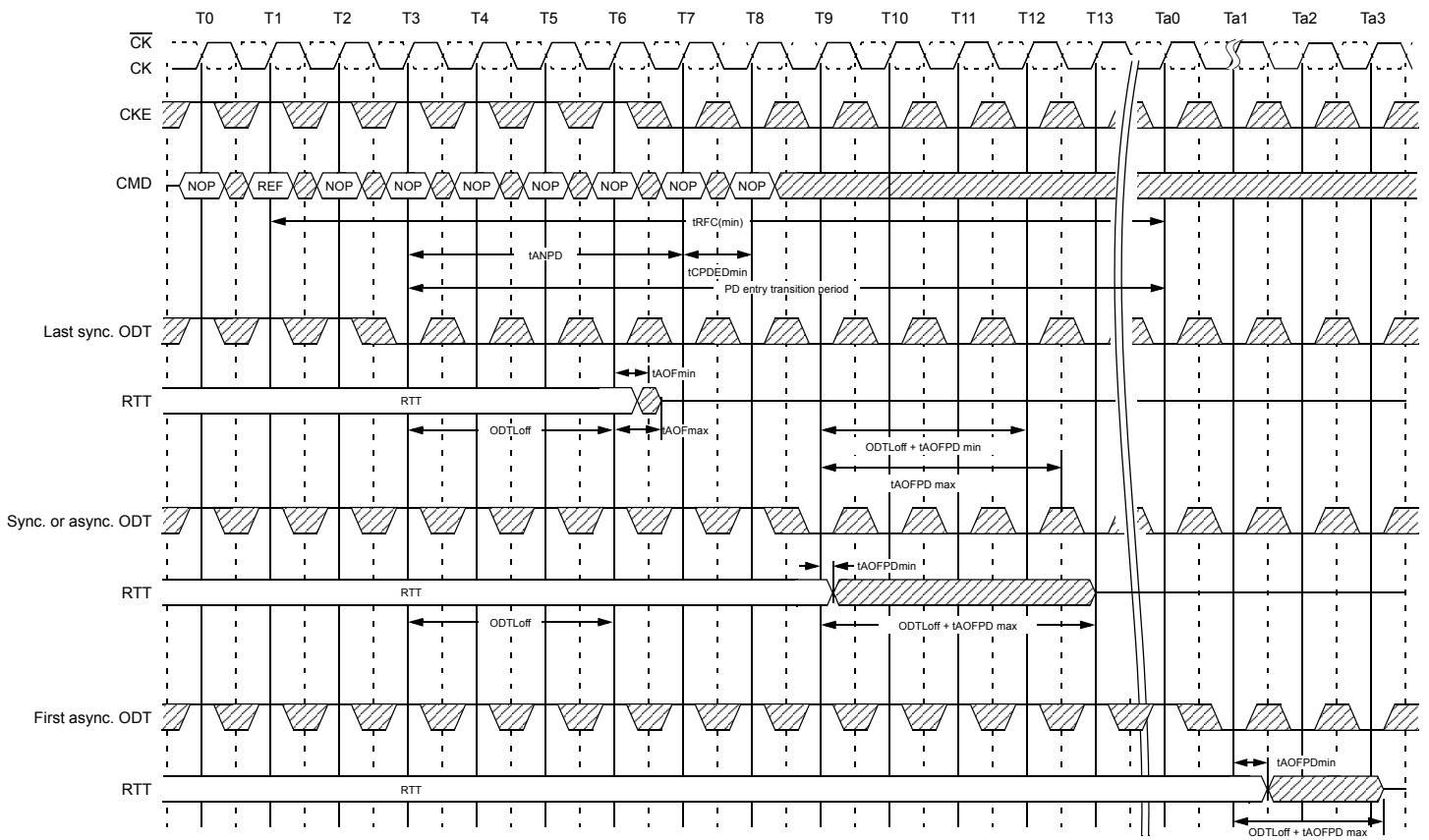


Figure 85. Synchronous to asynchronous transition after Refresh command (AL=0; CWL=5; tANPD=WL-1=4)

3.4.3 Asynchronous to Synchronous ODT Mode Transition during Power-Down Exit

If DLL is selected to be frozen in Precharge Power Down Mode by the setting of bit A12 in MR0 to "0", there is also a transition period around power down exit, where either synchronous or asynchronous response to a change in ODT must be expected from the DDR3 SDRAM. This transition period starts t_{ANPD} before CKE is first registered high, and ends t_{XPDLL} after CKE is first registered high. t_{ANPD} is equal to $\max\{ODT_{Loff}, ODT_{Lon}\}$ and is counted from the clock cycle where CKE is first registered high.

ODT assertion during the transition period may result in an RTT change as early as the smaller of $t_{AONPD \min}$ and $(ODT_{Lon} * t_{CK} + t_{AON \min})$ and as late as the larger of $t_{AOFPD \max}$ and $(ODT_{Lon} * t_{CK} + t_{AON \max})$. ODT de-assertion during the transition period may result in an RTT change as early as the smaller of $t_{AOFPD \min}$ and $(ODT_{Loff} * t_{CK} + t_{AOF \min})$ and as late as the larger of $t_{AOFPD \max}$ and $(ODT_{Loff} * t_{CK} + t_{AOF \max})$.

Note that, if AL has a large Value, the range where RTT is uncertain becomes quite large. Figure 86 shows the three different cases: ODT_C, asynchronous response before t_{ANPD} ; ODT_B has a state change of ODT during the transition period; ODT_A shows a state change of ODT after the transition period with synchronous response.

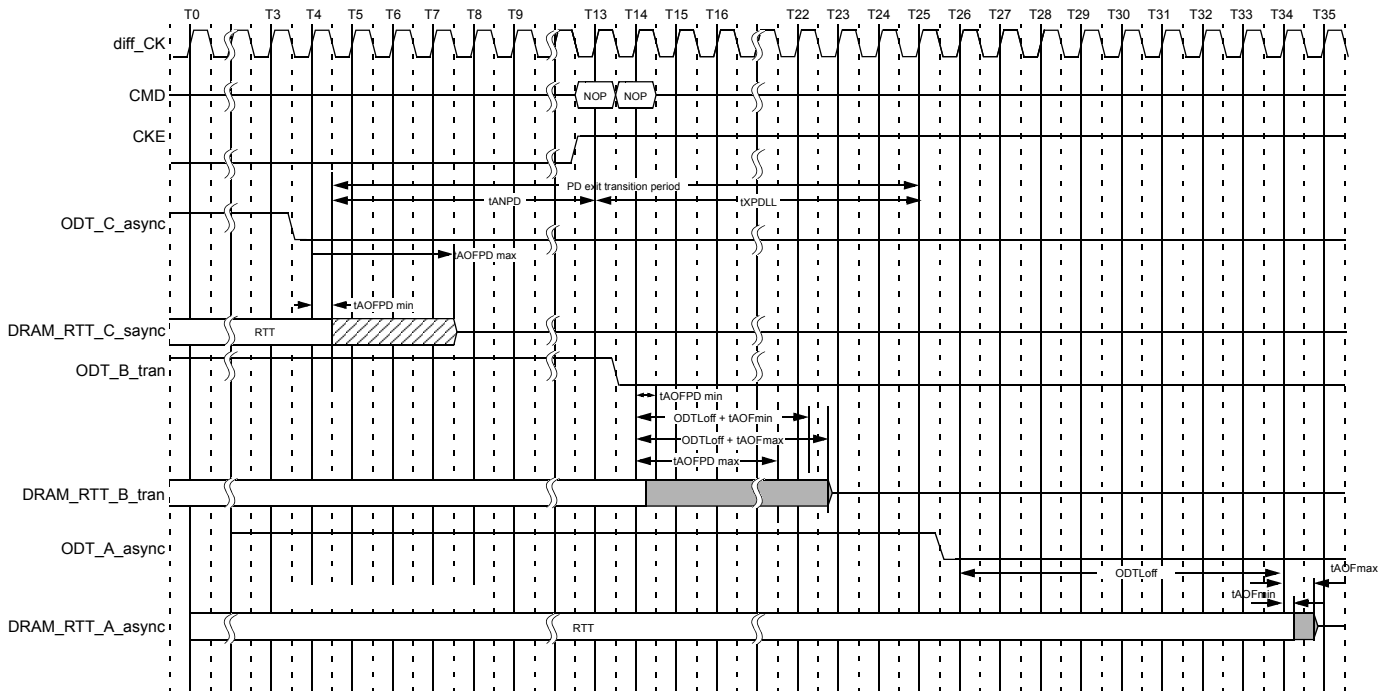


Figure 86. Asynchronous to synchronous transition during Precharge Power Down (with DLL frozen) exit (CL=6; AL=CL-1; CWL=5; $t_{ANPD}=WL-1=9$)

3.4.4 Asynchronous to Synchronous ODT Mode during short CKE high and short CKE low periods

If the total time in Precharge Power Down state or Idle state is very short, the transition periods for PD entry and PD exit may overlap. In this case the response of the DDR3 SDRAMs RTT to a change in ODT state at the input may be synchronous OR asynchronous from the start of the PD entry transition period to the end of the PD exit transition period (even if the entry period ends later than the exit period).

If the total time in Idle state is very short, the transition periods for PD exit and PD exit and PD entry may overlap. In this case the response of the DDR3 SDRAMs RTT to a change in ODT state at the input may be synchronous OR asynchronous from the start of the PD exit transition period to the end of the PD entry transition period. Note that, it is assumed that there was no Refresh command in progress when Idle state was entered.

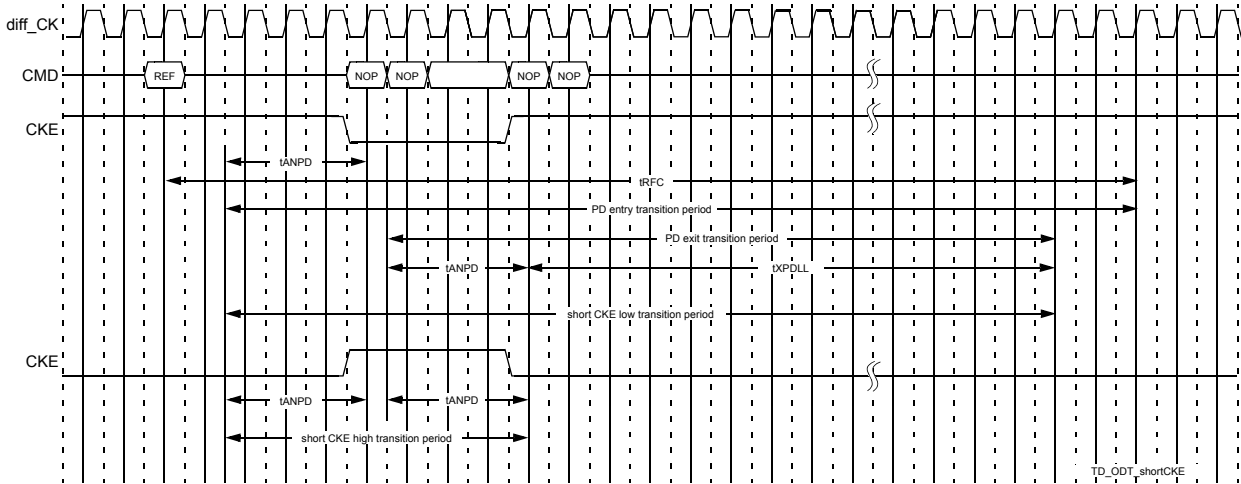


Figure 87. Transition period for short CKE cycles with entry and exit period overlapping
(AL=0, WL=5, $t_{ANPD}=WL-1=4$)