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CMM-B

CXL Memory Module - Box

White Paper

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Introduction

The CMM-B (CXL Memory Module - Box) is an advanced memory pooling solution designed for rack scale computing environments, utilizing Compute Express Link (CXL) technology to facilitate disaggregated, extensible, and composable memory architectures with enhanced software compatibility. The CMM-B enables flexible allocation of memory resources by supporting the connection of up to 8x E3.S CXL memory devices (CMM-D) to host systems. It is compatible with CXL1.1 and CXL 2.0 protocols, incorporating CXL SoC switch chip from Xconn. The CMM-B, a 4U rack-mountable system, was developed in collaboration with AIC for chassis design, and is capable of significantly scaling memory capacity and bandwidth. Its performance has been evaluated with industry leading SAP HANA IMDB application, demonstrating 32% improvement in TPC-DS performance through software interleaving with two Up Stream Ports (USPs) which connect seven Samsung CMM-D devices in CMM-B compared to a single USP configuration that connects one CMM-D device in CMM-B in addition to capacity scalability up to 1.75TB.

CMM-B overview

The CMM-B (CXL Memory Module - Box) facilitates both static and dynamic configuration through a Fabric Manager (FM), Samsung Cognos Management Console system managing operational states via Fabric Manager Application Programming Interface (FMAPI) commands aligned with the CXL specification. Currently, the CMM-B supports Single Logical Device (SLD) memory pooling as a part of CXL 2.0 specification. It treats the CXL switch as a singular virtual device that is recognized by the host through the Device-Specific Configuration Space (DVSEC) in the connected upstream port. This DVSEC details the size of devices bound in the downstream port.

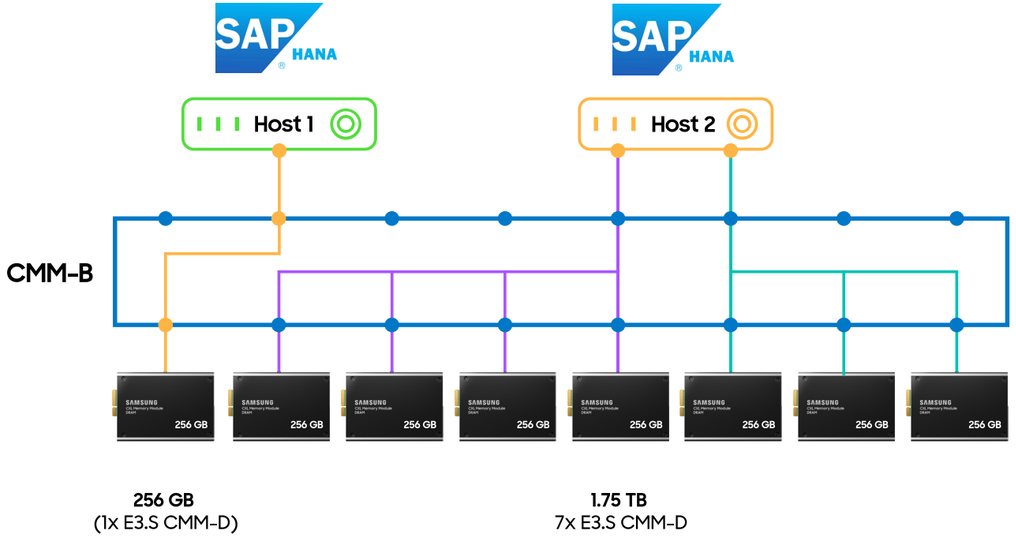
The validation platform for the CMM-B utilizes the Intel Emerald Rapid servers. The validation involved CMM-D devices, each with a configuration of PCIe Gen5 x8 and a capacity of 256GB. Performance assessments were conducted using the Intel Memory Latency Checker (MLC) to evaluate the CXL switch.

Evaluations were performed on PCIe Gen5 x8 upstream ports (USPs), with downstream ports (DSPs) set to PCIe Gen5 x8. The peak throughput recorded was 28GB/s, with an average of 19GB/s on the PCIe Gen5 x8 USP. Throughput variability was noted, influenced by the connection of the USP to the host socket and the execution location of the benchmark program. Specifically, throughput could achieve up to 28GB/s if the USP and all CXL DRAM-utilizing threads were on Socket 0, but it could decrease to 15GB/s if threads were executed on a different node, such as Socket 1. Latency also varied, with a minimum of 390ns and an average of 520ns. Without CPU affinity settings, throughput would average between 19GB/s and 20GB/s, as thread execution would be split between local and remote sockets.

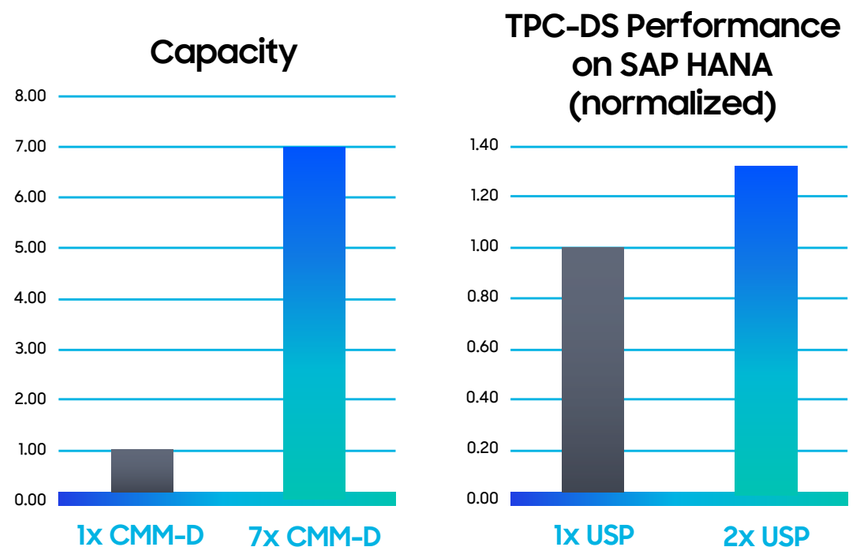
For multiple USPs use case performance evaluation, software (SW) interleaving was facilitated by 'numactl'. This assessment utilized two and three USPs for dual and triple SW interleaving configurations, respectively, on a single Emerald Rapid server. Notably, the Emerald Rapid architecture does not accommodate three CXL connections on a singular CPU socket, necessitating dual CPU sockets for the three USPs scenarios. Performance results indicated that dual SW interleaving achieved a throughput of up to 39 GB/s and an idle latency of 530ns, while triple SW interleaving reached up to 60 GB/s throughput and 596ns latency. These performance metrics are measured by loaded_latency and idle_latency option.

Regarding capacity, the CMM-B supports Single Logical Device (SLD) memory pooling, with up to 1:8 device binding capacity allowing for the connection of eight CMM-D devices to a single USP, enabling up to 2TB connection per USP. Despite the lack of hardware interleaving support, this configuration facilitates capacity scaling on a singular port. Evaluations were conducted across various scenarios involving three USPs and eight DSPs on two Emerald Rapid servers, demonstrating the system's capability to enhance memory capacity effectively.

A Demonstration Use Case: SAP HANA In-Memory Database



In our demo scenario, the integration and validation of the CMM-B were successfully completed with SAP HANA database. Despite SAP HANA's lack of native support for CXL memory, it can utilize DAX-enabled devices for its main storage. As we discussed in the previous section, the memory capacity scales as more CMM-D devices are attached to a host. To evaluate performance across multiple CXL devices, configurations like NUMA interleaving and Device Mapper striping were applied. SAP HANA throughput improvements were measured using the TPC-DS benchmark with 16 client threads. The findings revealed that employing NUMA interleaving with two USPs led to 32% performance boost over a single USP setup. A single USP connects to a single CMM-D device (256GB) and two UPS configuration connects to seven CMM-D devices (1.75TB).



Summary

CMM-B provides support for CXL memory pooling functionality. It currently enables the integration of CMM-D devices with capacities up to 2TB with 8x E3.S CMM-D devices and supports up to three hosts with the ability to scale their capacity and bandwidth. We evaluated memory capacity and bandwidth scalability on multiple scenarios and also demonstrated that memory intensive application such as SAP HANA could achieve big performance benefit as more CXL memory bandwidth is attached.

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